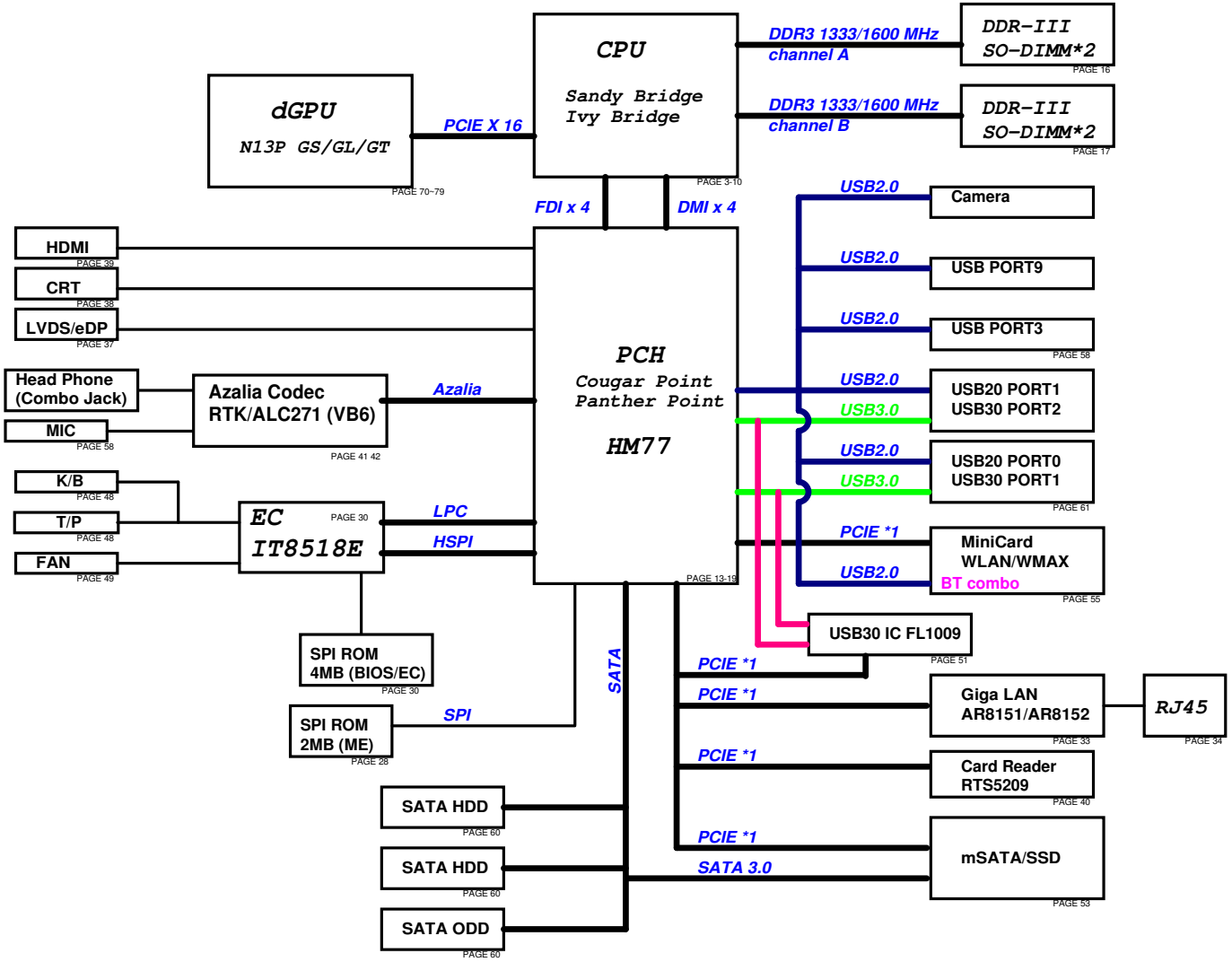
VA70 BLOCK DIAGRAM



POWER

CPU VCORE PAGE 80
SYSTEM, +3V, +5V PAGE 81
+VCCP & +VCCP_VT PAGE 82
DDR & VTT PAGE 83
2.5V & 1.5VS &1.1VS PAGE 84
SMART CHARGER PAGE 88
POWER DETECT PAGE 90
LOAD SWITCH PAGE 91
POWER PROTECT PAGE 92

VGA POWER

GPU VCORE PAGE 80
+1.05VS_VGA
+1.5VS_VGA
+3VS_VGA
+12VS_VGA
LOAD SWITCH PAGE 91
POWER PROTECT PAGE 92

Power Rails

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

PCIe Port

PCIE_P1	CARDREADER
PCIE_P2	Mini CARD (WLAN)
PCIE_P3	mSATA
PCIE_P4	USB30
PCIE_P5	
PCIE_P6	LAN

USB20 PORT

USB P00	External MB
USB P01	External MB
USB P02	
USB P03	External DB
USB P04	
USB P05	BT
USB P08	Camera
USB P09	External DB
USB P10	
USB P11	SSD
USB P12	
USB P13	

SATA PORT

SATA P0	HDD 1
SATA P1	HDD 2
SATA P2	ODD 3
SATA P3	mSATA
SATA P4	
SATA P5	

IO BOARD

- USB PORT3
- USB PORT9
- HP_OUT
- MIC IN

TP BT BOARD

- Touch PAD Button
- LID SW

PWR BOARD

- POWER Button
- POWER LED
- LID SW

PEGATRON Title : BLOCK DIAGRAM

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size: Custom | Project Name: BA52HR/CR | Rev: 1.0

Date: Friday, February 03, 2012 | Sheet 1 of 77

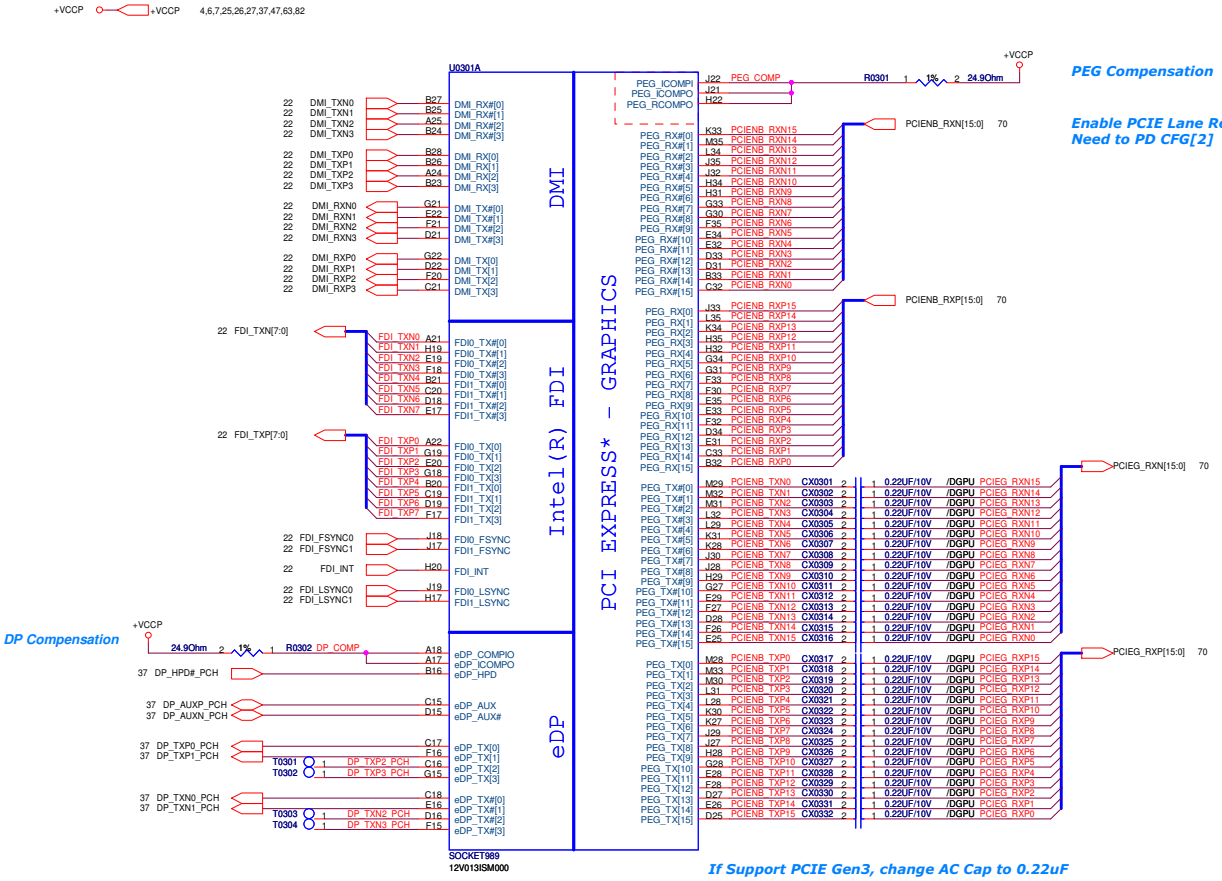
BOM optional	Remark
N/A	For 上件
/ABCT	For ABCT，上件
/niAMT	For no iAMT，上件
/HOME	For 上件
/HR	For Huron River，上件
/Non_HSPI	For ROM SETTING ，上件
Entry	For 上件
Main	For 上件
/USB20	For USB 2.0 ，上件
/HSPI	For 不上件
/HDMI	For HDMI用，不上件
/TP1_AUD	For power control，不上件
/TP1_BT	For power control，不上件
/TP1_CAMERA	For power control，不上件
/TP1_CR	For power control，不上件
/TP1_LAN	For power control，不上件
/TP1_ODD	For power control，不上件
/TP1_WLAN	For power control，不上件
/THERM	For Palm Rest溫度，不上件
/usb30	For USB 3.0 ，不上件
/ZPODD	For ODD battery saving使用Mount R5108，不上件
@	For 不上件
@/MP	For debug port, MP不上件
/BT270	視keypat list而定
/COMBO_BT	視keypat list而定
/SATA+	For Sata Repeater, SR先上件

PEGATRON Title : System Setting

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
A	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 2 of 94



Title :	CPU(1)_DMI,PEG,FDI,CLK,MISC
PEGATRON COMPUTER INC	Engineer: Wing_Cheng
Size: C	Project Name: BA52HR/CR
Rev: 1.0	
Date: Friday, February 03, 2012	Sheet 3 of 94

Select the termination voltage of DMI and FDI Tx/Rx (PCH Strap)
H_SNB_IVB# connected to DF_TVS via 1Kohm
DF_TVS needs PU via 2.2Kohm to +1.8VS

U0301B

MISC
SNB_IVB#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#

CLOCKS
BCLK
BCLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#

THERMAL
DDR3 MISC
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]

PWR MANAGEMENT
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#

JTAG & BPM
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]

SOCKET989
12V013ISM000

do not remove because POWER removed thier PU R. Joyoung0613

R1.0 1229

DDR3 DRAM Reset.

System Memory Impedance Compensation
Huron River platform Design Guide 436735 P.88 Table 37.
Eric Fang to Alan Chien 11/15/2010

Huron River platform Design Guide Update 440484
SM_RCOMP_1 use 26ohm 1%

R1.0 PU/PD for JTAG signals

PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ

R1.1 change to short pin

1.57 Volt

Vcc=1.65-5.5

Power good for +1.5V_VCCDDQ (delay > 100ns)

Reserve S3 power reduction schematic

If don't support S3 power reduction
1. Unmount R0450, R0452, U0404, R0453, Q0403, C0404, R0455, R0454, C0405
2. Change R0449 to 200ohm from 1kohm, change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106

3. Unmount Q0501, C0501, R0506, R0504, R0507
4. Mount R0501, change r0508 to 0ohm from 1kohm

5 Unmount Q0701, R0703, R0705, Q0702
6. Mount R0702 and short JP0701

7. Unmount R2232, R2231, Q2203

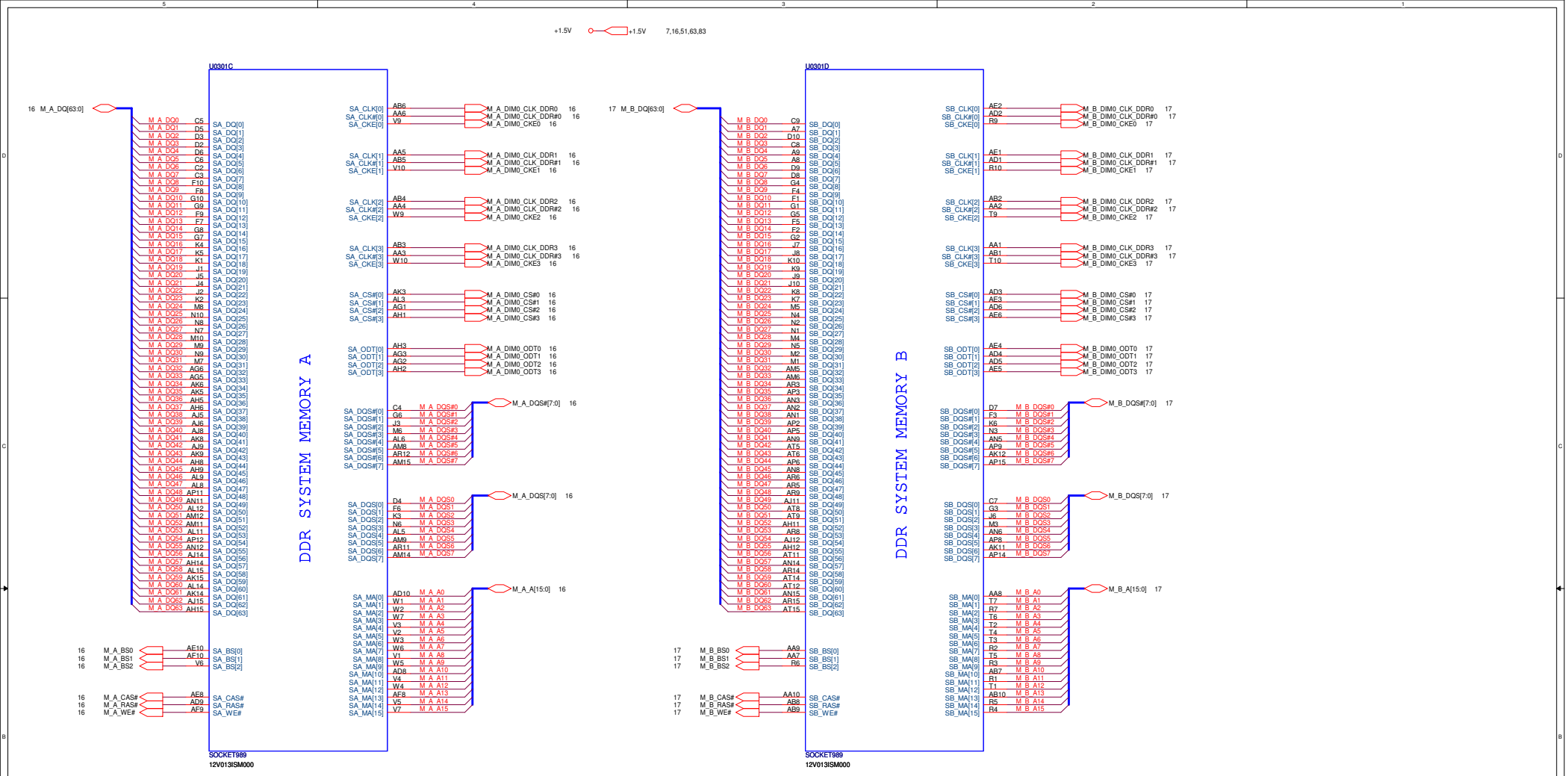
Check Frank remove or not??

R1.0 0119
Sandy Bridge:R0417 = 750 ohm (10V220000093)
Ivy Bridge:R0417 = 680 ohm (10V240000041)

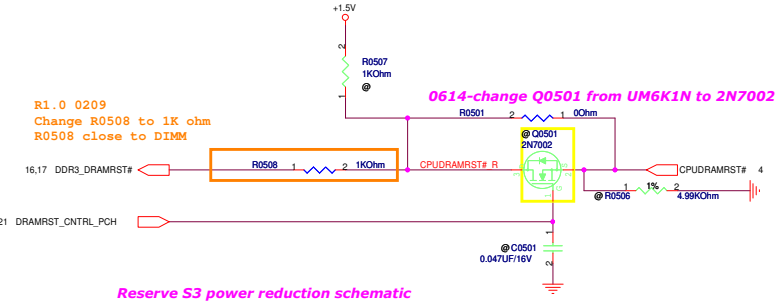
Frank
0506 EVERST check

R1.0 0224
Intel Comments

PEGATRON	Title :	CPU(1)_DMI,PEG,FDI,CLK,MISC	
PEGATRON COMPUTER INC	Engineer:	Wing_Cheng	
Size: C	Project Name: BA52HR/CR		Rev: 1.0
Date: Friday, February 03, 2012	Sheet 4 of 94		



R1.0 S3 circuit:- DRAM_RST# to memory should be high during S3



Reserve S3 power reduction schematic

If don't support S3 power reduction
1. Unmount R0450, R0452, U0404, R0453, Q0403, C0404, R0455, R0454, C0405
2. Change R0449 to 200ohm from 1kohm, change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106

3. Unmount Q0501, C0501, R0506, R0504, R0507
4. Mount R0501, change r0508 to 0ohm from 1kohm

5 Unmount Q0701, R0703, R0705, Q0702
6. Mount R0702 and short JP0701

7. Unmount R2232, R2231, Q2203

PEGATRON Title : CPU(2)_DDR3

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 5 of 94

POWER

Vcc for processor core
Voltage range: 0.3 - 1.52V

Voltage for the memory controller and shared cache defined at the motherboard VCCIO_SENSE and VSS_SENSE_VCCIO

SV-QC ICCMAX 94A
SV-DC ICCMAX 53A

ICCMAX_VCCIO 8.5A

U0301F

+VCORE — Check net name??

+VCCP — Check net name??

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

R1.0 0126
Intel Comments

R1.0 0126
Intel Comments

R1.0 0126
Intel Comments

0614-Remove C0641 and nostuff C0651,C0647,C0658

0622-Remove CE0603(powre schematic reserve)

0622-Remove CE0601(powre schematic reserve)

+VCCP +VCCP 3,4,7,25,26,27,37,47,63,82
+VCORE +VCORE 63,80

Check net name??

HR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

EIH31/30 (EE)
+VCCP 10uF * 19pcs (2pcs no stuff)
22uF* 10 pcs (total no stuff)
330 uF *1pcs Power support

CR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

Decoupling guide for Everest (EE)
+VCCP 22uF * 19pcs (7 no stuff)
330uF * 1pcs (1 no stuff)=>JE31HR/CR power support

HR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

EIH31/30
+VCC_CORE 22uF * 14pcs(6pcs unmount)
10uF * 16pcs (4pcs unmount)
470uF * 2pcs (Power support)

CR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

Decoupling guide for Everest (EE)
+VCC_CORE 22uF * 16pcs (8 nostuff)
10uF * 10pcs (3 nostuff)
470uF * 1pcs=>JE31HR/CR power support

Frank
20110602 check pull up/pull down reserve power schematic or not.

Frank
20110516 Change VCCP_SENSE to VCCIO_SENSE and change VSSP_SENSE to VSSIO_SENSE for meet power schematic.

Frank
20110516 Remove R0601 and R0604, because Power is already reserved

SOCKET989
12V013ISM000

PEGATRON	Title :	CPU(4)_PWR
PEGATRON COMPUTER INC	Engineer:	Wing_Cheng
Size: C	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, February 03, 2012	Sheet 6 of 94	

SV-QC ICCMAX_VAXG 33A
SV-DC ICCMAX_VAXG 33A

POWER

R1.0 Add net name. Joyoung 0621

0614-Add SP0701,SP0702

Close to CPU

+VGFX_CORE

Graphics core voltage
Voltage range: 0 ~ 1.52V

C0703 22UF/6.3V, C0704 22UF/6.3V, C0705 22UF/6.3V, C0706 22UF/6.3V, C0707 22UF/6.3V, C0708 22UF/6.3V
C0711 22UF/6.3V, C0712 22UF/6.3V, C0713 22UF/6.3V, C0714 22UF/6.3V, C0715 22UF/6.3V, C0716 22UF/6.3V

0622-Remove CE0705(powre schematic reserve)

HR_Decoupling guide from Intel (POWER + EE)
+VGFX_CORE 22uF * 12pcs
470uF * 2pcs

EIH31/30
+VCCP 22uF* 16 pcs (6 unmount)
330uF * 1pcs (power support)
470uF *1pcs (EIH31 Del 470uF For Layout)

CR_Decoupling guide from Intel (POWER + EE)
+VGFX_CORE 22uF * 12pcs
470uF * 2pcs

Decoupling guide for Everest (EE)
+VGFX_CORE 22uF * 12pcs (2 nostuff)
470uF * 1pcs (JE31HR/CR power support)

PLL supply voltage (DC + AC specification)

ICCMAX_VCCPLL 1.2A

+1.8VS
CE0701 220UF/6.3V 1BV090000003, C0717 10UF/6.3V, C0718 1UF/6.3V, C0719 1UF/6.3V

HR_Decoupling guide from Intel (POWER + EE)
+1.8VS 1uF * 2pcs
10uF * 1pcs
330uF * 1pcs

EIH31/30
+1.8VS 1uF * 2pcs
10uF * 1pcs
2.2uF*1pcs
4.7uF*1pcs
22uF * 1pcs (un-mount)

CR_Decoupling guide from Intel (POWER + EE)
+1.8VS 1uF * 2pcs
10uF * 1pcs
330uF * 1pcs

Decoupling guide from Everest (EE)
+1.8VS 1uF * 2pcs
10uF * 1pcs
100uF * 1pcs

U0301G

SENSE LINES
VAXG_SENSE AK35
VSSAXG_SENSE AK34
VCCGT_SENSE_R SP0701 R0402
VSSGT_SENSE_R SP0702 R0402
VCCGT_SENSE 80
VSSGT_SENSE 80

VREF
SM_VREF AL1
+V_SM_REF 10mil
+V_SM_REF_CNT
R0702 0Ohm
Q0701 SI2308DS-T1-E3
R0703 100KOhm
+V_SM_VREF

DDR3 Reference Voltage

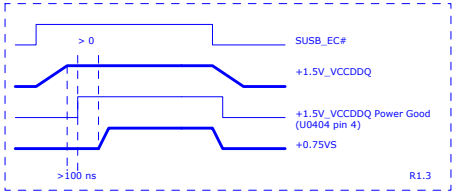
Reserve S3 power reduction schematic

DDR3 -1.5V RAILS
VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1
C0725 10UF/6.3V, C0724 10UF/6.3V, C0723 10UF/6.3V N/A, C0722 10UF/6.3V, C0721 10UF/6.3V N/A, C0720 10UF/6.3V N/A, CE0702 220UF/6.3V
+1.5V_VCCDDQ
PS_S3CNTRL_1.5V_R
R0705 0Ohm
C0730 470PF/50V
PS_S3CNTRL_1.5V 22
Q0702 SI4336DY_T1_E3
+1.5V
3MM_OPEN_5MIL JP0701

ICCMAX_VDDQ 5A Joyoung 0613
Reduce to 5A (EDS R2.1)

Processor I/O supply voltage for DDR3 (DC + AC specification)

0614-Change JP(3MM_OPEN_5MIL)



HR_Decoupling guide from Intel (POWER + EE)
+VDDQ 10uF * 6pcs
330uF * 1pcs

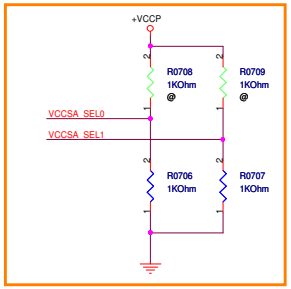
EIH31
+VDDQ 10uF * 6pcs (3 nostuff)
220uF * 1pcs

CR_Decoupling guide from Intel (POWER + EE)
+VDDQ 10uF * 6pcs
330uF * 1pcs

Decoupling guide for Everest (EE)
+VDDQ 10uF * 6pcs (3 nostuff)
220uF * 1pcs

SA RAIL
ICCMAX_VCCSA 6A
Voltage for the System Agent and VCCSA_SENSE
0614-Remove C0728
+VCCSA
VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25
C0729 10UF/6.3V, C0727 10UF/6.3V, C0726 10UF/6.3V N/A, CE0703 100UF/6.3V
VCCSA_SENSE H23
R0704 0Ohm Close to CPU
VCCSA_SENSE 85
FC_C22 C22
VCCSA_VID1 C24
VCCSA_SEL0 85
VCCSA_SEL1 85
R1.0 0101

MISC
R1.0 0209
Intel Comments



+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

HR_Decoupling guide from Intel (POWER + EE)
+VCCSA 10uF * 3pcs
330uF * 1pcs

EIH31/30
+VCCSA 10uF * 4pcs (2 nostuff)
100uF * 1pcs

CR_Decoupling guide from Intel (POWER + EE)
+VCCSA 10uF * 3pcs
330uF * 1pcs

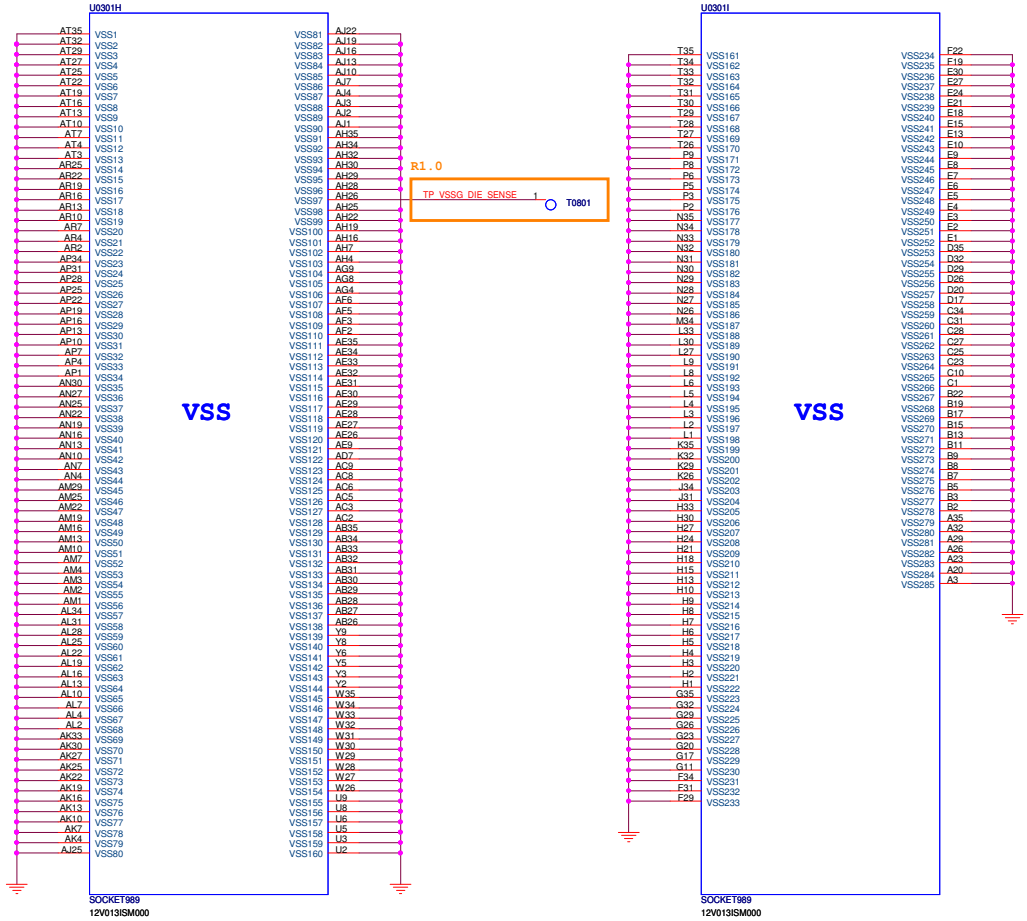
Decoupling guide for Everest (EE)
+VCCSA 10uF * 3pcs (1 nostuff)
100uF * 1pcs

1.8V RAIL
SOCKET989
12V013ISM000
VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

GRAPHICS
VAXG1 AT24
VAXG2 AT23
VAXG3 AT21
VAXG4 AT20
VAXG5 AT18
VAXG6 AT17
VAXG7 AR24
VAXG8 AR23
VAXG9 AR21
VAXG10 AR20
VAXG11 AR18
VAXG12 AR17
VAXG13 AP24
VAXG14 AP23
VAXG15 AP21
VAXG16 AP20
VAXG17 AP18
VAXG18 AP17
VAXG19 AN24
VAXG20 AN23
VAXG21 AN21
VAXG22 AN20
VAXG23 AN18
VAXG24 AN17
VAXG25 AM24
VAXG26 AM23
VAXG27 AM21
VAXG28 AM20
VAXG29 AM18
VAXG30 AM17
VAXG31 AL24
VAXG32 AL23
VAXG33 AL21
VAXG34 AL20
VAXG35 AL18
VAXG36 AL17
VAXG37 AK24
VAXG38 AK23
VAXG39 AK21
VAXG40 AK20
VAXG41 AK18
VAXG42 AK17
VAXG43 AJ24
VAXG44 AJ23
VAXG45 AJ21
VAXG46 AJ20
VAXG47 AJ18
VAXG48 AJ17
VAXG49 AH24
VAXG50 AH23
VAXG51 AH21
VAXG52 AH20
VAXG53 AH18
VAXG54 AH17

+VCCP +VCCP 3,4,6,25,26,27,37,47,63,82
+1.5V +1.5V 5,16,51,63,83
+VCCSA +VCCSA 85
+1.8VS +1.8VS 25,26,63,84
+VGFX_CORE +VGFX_CORE 63,80
+1.5V_VCCDDQ +1.5V_VCCDDQ 4
+V_SM_VREF +V_SM_VREF 18

PEGATRON Title : CPU(4)_PWR
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, February 03, 2012 | Sheet 7 of 94



PEGATRON	Title :	CPU(3)_CFG,RSVD,GND	
PEGATRON COMPUTER INC	Engineer:	Wing_Cheng	
Size: C	Project Name: BA52HR/CR		Rev: 1.0
Date: Friday, February 03, 2012	Sheet 8 of 94		

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection

- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training

R1.0
Add CFG0

Frank
0516 Remove CFGO to XDP

U0301E

TPC26T T0918 CFG0 AK28 CFG[0]
TPC26T T0917 CFG1 AK29 CFG[1]
TPC26T T0916 CFG2 AL26 CFG[2]
TPC26T T0915 CFG3 AL27 CFG[3]
TPC26T T0914 CFG4 AK26 CFG[4]
TPC26T T0913 CFG5 AL29 CFG[5]
TPC26T T0912 CFG6 AL30 CFG[6]
TPC26T T0911 CFG7 AM31 CFG[7]
TPC26T T0910 CFG8 AM32 CFG[8]
TPC26T T0909 CFG9 AM30 CFG[9]
TPC26T T0908 CFG10 AM28 CFG[10]
TPC26T T0907 CFG11 AM26 CFG[11]
TPC26T T0906 CFG12 AN28 CFG[12]
TPC26T T0905 CFG13 AN31 CFG[13]
TPC26T T0904 CFG14 AN26 CFG[14]
TPC26T T0903 CFG15 AM27 CFG[15]
TPC26T T0902 CFG16 AK31 CFG[16]
TPC26T T0901 CFG17 AN29 CFG[17]

TPC26T T0953 VAXG_VAL_SENSE AJ31 RSVD1
TPC26T T0952 VSSAXG_VAL_SENSE AH31 RSVD2
TPC26T T0951 VCC_VAL_SENSE AJ33 RSVD3
TPC26T T0950 VSS_VAL_SENSE AH33 RSVD4
AJ26 RSVD5
B4 RSVD6
D1 RSVD7
F25 RSVD8
F24 RSVD9
F23 RSVD10
D24 RSVD11
G25 RSVD12
G24 RSVD13
E23 RSVD14
D23 RSVD15
C30 RSVD16
A31 RSVD17
B30 RSVD18
B29 RSVD19
D30 RSVD20
B31 RSVD21
A30 RSVD22
C29 RSVD23
J20 RSVD24
B18 RSVD25
A19 RSVD26
J15 RSVD27

RESERVED

RSVD28 L7
RSVD29 AG7
RSVD30 AE7
RSVD31 AK2
RSVD32 W8
RSVD33 AT26
RSVD34 AM33
RSVD35 AJ27
RSVD37 T8
RSVD38 J16
RSVD39 H16
RSVD40 G16
RSVD41 AR35
RSVD42 AT34
RSVD43 AT33
RSVD44 AP35
RSVD45 AR34
RSVD46 B34
RSVD47 A33
RSVD48 A34
RSVD49 B35
RSVD50 C35
RSVD51 AJ32
RSVD52 AK32
RSVD53 AH27 TP_VCCG_DIE_SENSE 1 T0954 TPC26T
RSVD54 AN35
RSVD55 AM35
RSVD56 AT2
RSVD57 AT1
RSVD58 AR1
KEY B1

SOCKET989
12V013ISM000

CFG2 R0902 /DGPU 1% 1KOhm
CFG4 R0903 1% 1KOhm
CFG5 R0904 1% @ 1KOhm
CFG6 R0905 1% @ 1KOhm
CFG7 R0906 1% @ 1KOhm

This model is UMA, unmount R0902(use Default)

DDR_WR_VREF01
DDR_WR_VREF02

R1.0 0126
R0909 1KOhm 1% @
R0910 1KOhm 1% @

DIMM0_VREF_DQ_R Pull Down 1k ohm
DIMM1_VREF_DQ_R Pull Down 1k ohm
Design Guide 1.0 P.89 Figure 44 (436735)

Power schematic reserve 1.0V or not??

+VCCIO_SEL	
1	1.05V
0	1.00V

IVB VCCIO for Mobile and Desktop is changed from 1.0v to 1.05v, same as PPT VCCIO. (461017 WW23'11)

R1.0 0111
Delete VCCIO_SEL. Joyoung0614
TPC26T T0955 VCCIO_SEL_R

Frank
20110516 Change VCCP_SEL to VCCIO_SEL for meeting Power schematic defined

PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:

R0911 @ 0Ohm
@ Q0901A UM6K1N
DDR_WR_VREF01 → DIMM0_VREF_DQ 18
5,21 DRAMRST_CNTRL_PCH

M3 Path:0 Ohm at Page18

R0912 @ 0Ohm
@ Q0901B UM6K1N
DDR_WR_VREF02 → DIMM1_VREF_DQ 18

Reserve S3 power reduction schematic

M3: Processor Generated SO-DIMM VREFDQ
– New Requirement

Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

PEGATRON Title : CPU(3)_CFG,RSVD,GND
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, February 03, 2012 | Sheet 9 of 94

+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27

+3VSUS +3VSUS 4,22,24,27,28,30,33,65,81,85,92

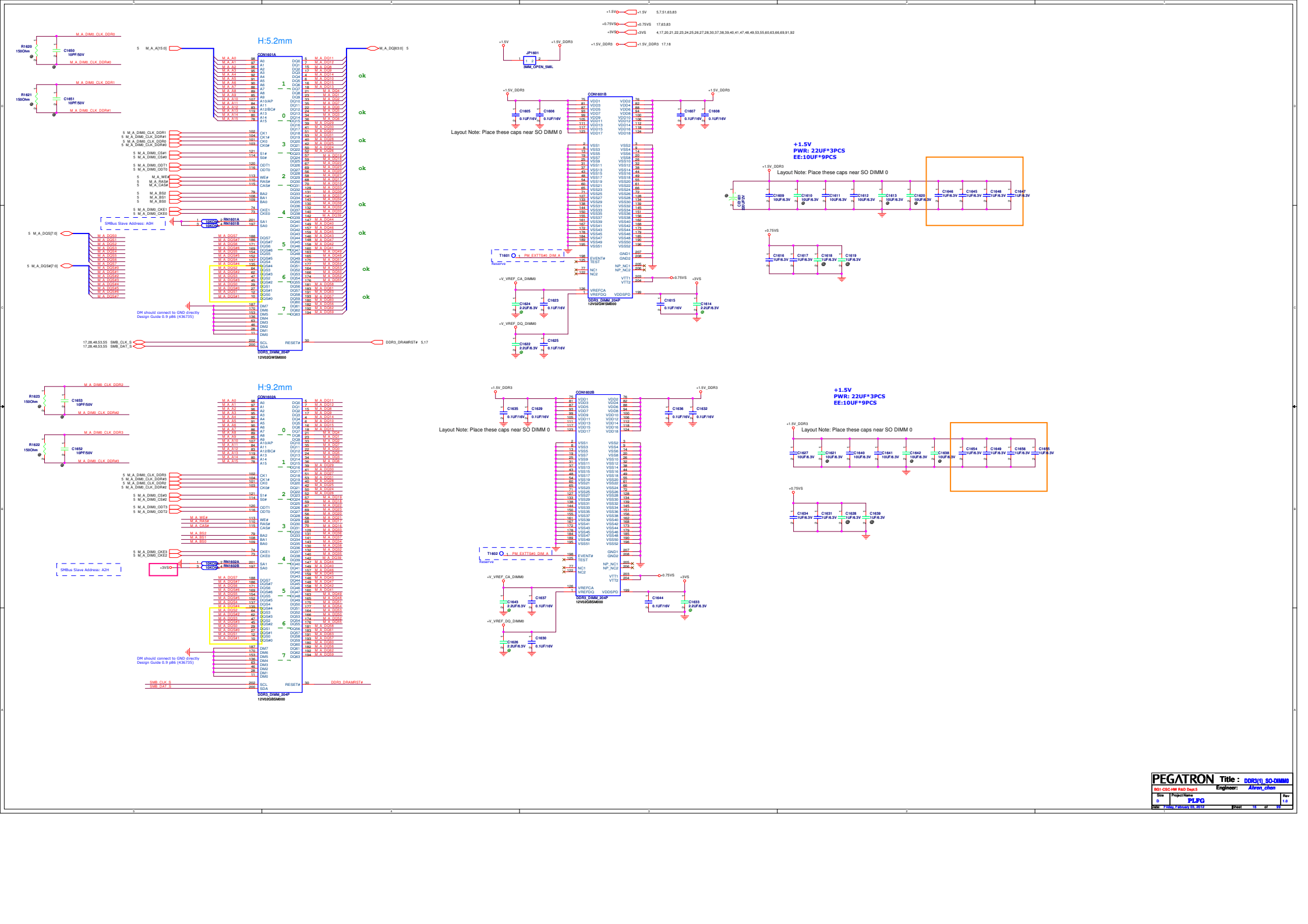
+VCCP +VCCP 3,4,6,7,25,26,27,37,47,63,82

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92

CPU XDP connector

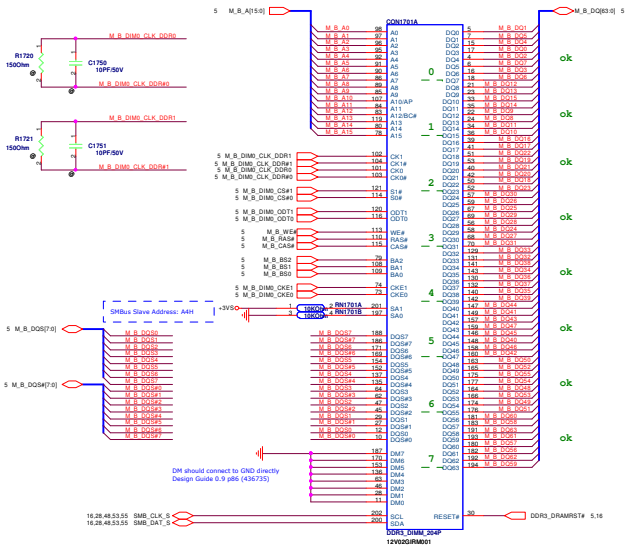
PCH XDP connector

PEGATRON	Title : NB(3)_****		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size: C	Project Name: BA52HR/CR		Rev: 1.0
Date: Friday, February 03, 2012	Sheet 10 of 99		

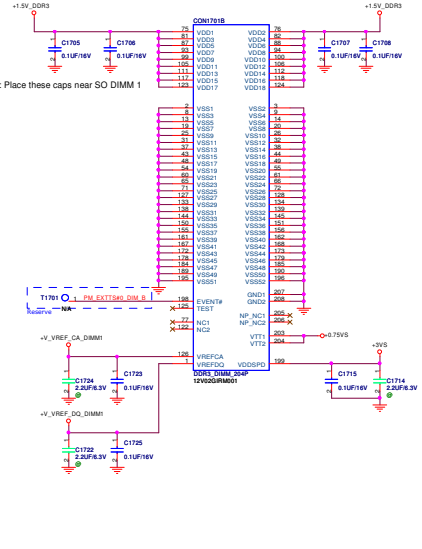


Title :	DDR3(1)_SO-DIMM0	
Engineer:	Ahren_chen	
Size	Project Name	Rev
D	PLFG	1.0
Date: Friday, February 03, 2012	Sheet 16 of 99	

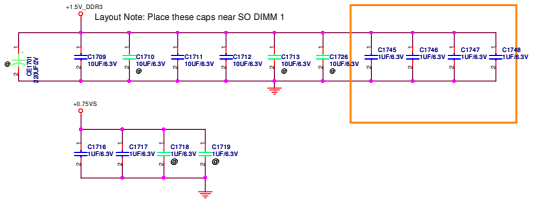
H:4MM



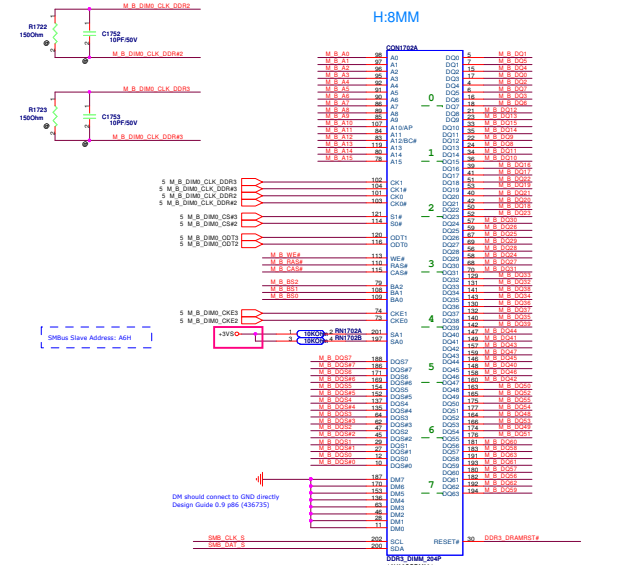
Layout Note: Place these caps near SO DIMM 1



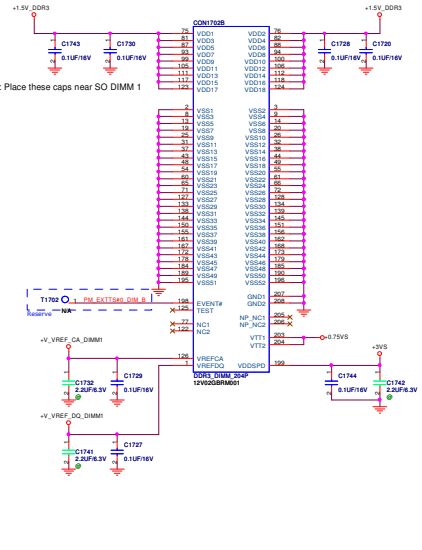
+1.5V
PWR: 22UF*3PCS
EE:10UF*9PCS



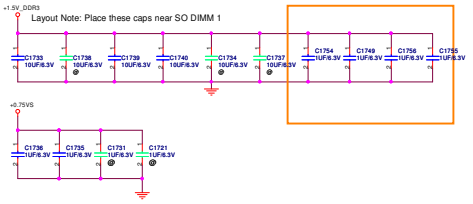
H:8MM



Layout Note: Place these caps near SO DIMM 1



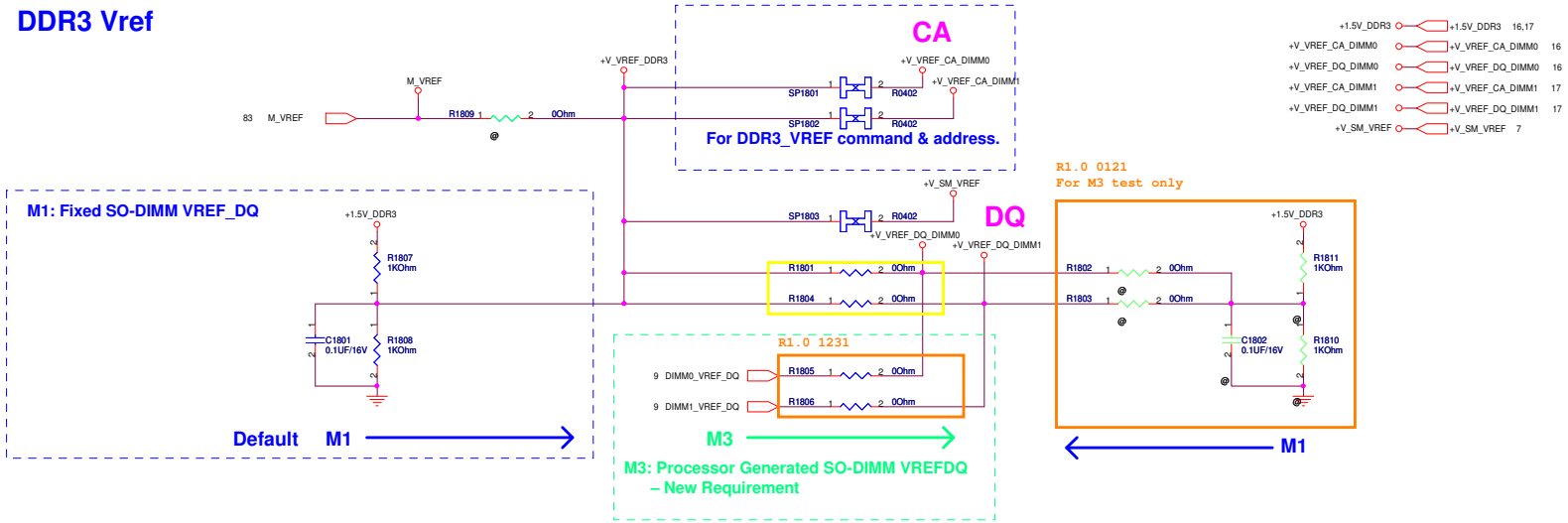
+1.5V
PWR: 22UF*3PCS
EE:10UF*9PCS



PEGATRON	Title :	DDR3(2)_SO-DIMM1	
801-2SC-HR R&D Dept.5	Engineer:	Alvren_chen	
Size: D	Project Name: PLPG		Rev: 1.0
Date: Friday, February 03, 2012	Sheet 17 of 99		

1202-000R000
(12V02GIRM001)

DDR3 Vref



If support M1 :(Sandy Bridge CPU Only)
1. Un mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Mount R1801,R1804
==>CA and DQ are the same path

If support M1 and M3 :(Sandy Bridge/Ivy Bridge CPU)
1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804
==> CA and DQ are separate path

Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

PEGATRON Title : DDR3(3)_CA/DQ Voltage
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, February 03, 2012 Sheet 18 of 94

R1.4--2

PEGATRON	Title : VID Controller	
PEGATRON COMPUTER INC	Engineer: Wing_Cheng	
Size: C	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, February 03, 2012	Sheet 19 of 94	

RTC battery

+RTCBAT — R2001 1KOhm — +RTC_BAT — D2001 1V/0.2A — +VCC_RTC — C2003 1UF/6.3V — GND

J2001 BATT_HOLDER_2P

R1.0 0110
增加點膠點

12V20GBSM000

Connector Type 1217-001L000

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

+VCC_RTC — RTCRST# RC delay should be 18ms~25ms

R2003 20KOhm — C2004 1UF/6.3V — JRST2001 SGL_JUMP @ — GND

R2004 20KOhm — C2005 1UF/6.3V — JRST2002 SGL_JUMP @ — R2005 1MOhm — GND

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

PCH_INTVRMEN — R2030 @ 200KOhm 1% — GND

ACZ_BCLK_AUD — C2010 10PF/50V

EMI solution

+VCC_RTC — +VCC_RTC 22,27

R1.0 Delete +RTCBAT

+3VA — +3VA 27,30,48,63,65,81,88,93

+3VS — +3VS 4,16,17,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92

+3VSUS_ORG — +3VSUS_ORG 21,22,24,25,27

+1.05VM_ORG — +1.05VM_ORG 27

+VTT_PCH_VCCIO — +VTT_PCH_VCCIO 26,27

C2001 15PF/50V — RTC_X1_C — SP2005 — R0402 — X2001 32.768KHZ — R2002 10MOhm — C2002 15PF/50V — GND

T2015 — T2011 — T2012

U2001A

RTC_X1	A20	RTCX1	RTC
RTC_X2	C20	RTCX2	
RTC_RST#	D20	RTCRST#	
SRTC_RST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	

+VCC_RTC — 330KOhm 1% — R2006

41 ACZ_BCLK_AUD	R2051 33Ohm	ACZ_BCLK	N34
41 ACZ_SYNC_AUD	R2052 33Ohm	ACZ_SYNC	L34
41 SB_SPKR		SPKR	T10
41,42 ACZ_RST#_AUD	R2055 33Ohm	ACZ_RST#	K34
41 ACZ_SDIN0_AUD		HDA_SDIN0	E34
Remove TP		HDA_SDIN1	G34
		HDA_SDIN2	C34
		HDA_SDIN3	A34
30 PCH_FLASH_DESCRIPTOR	R2050 @ 0Ohm		
41 ACZ_SDOUT_AUD	R2053 0Ohm	ACZ_SDOUT	A36
30 MEFLSH_EN#	R2054 @ 0Ohm	HDA_DOCK_EN#/GPIO33	C36
T2002		CARDREADER_RESET	N32

R2050 near R2008

HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDO, HDA_DOCK_RST#/GPIO13 — IHDA

T2024	PCH_JTAG_TCK_BUF	JTAG_TCK	J3
T2025	PCH_JTAG_TMS	JTAG_TMS	H7
T2026	PCH_JTAG_TDI	JTAG_TDI	K5
T2027	PCH_JTAG_TDO	JTAG_TDO	H1

JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO — JTAG

28,30 PCH_SPICLK		SPI_CLK	T3
28 PCH_SPICS0#		SPI_CS0#	Y14
28,30 PCH_SPICS1#	PCH_SPICS1#	SPI_CS1#	T1
28,30 PCH_SPISI		SPI_MOSI	V4
28,30 PCH_SPISO		SPI_MISO	U3

SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO — SPI

COUGAR_POINT_ES1
02V000000001

FWH0/LAD0	C38	LPC_AD0	30,65
FWH1/LAD1	A38	LPC_AD1	30,65
FWH2/LAD2	B37	LPC_AD2	30,65
FWH3/LAD3	C37	LPC_AD3	30,65
FWH4/LFRAME#	D36	LPC_FRAME#	30,65
LDRQ0#	F36	SNN_PCH_DRQ#0 — T2032	
LDRQ1#/GPIO23	K36	SNN_LPC_DRQ#1 — T2033	
SERIRQ	V5	Serial Interrupt Request	INT_SERIRQ 30,65

LPC

SATA 6G

SATA0RXN	AM3	SATA_RXN0	60
SATA0RXP	AM1	SATA_RXP0	60
SATA0TXN	AP7	SATA_TXN0	60
SATA0TXP	AP5	SATA_TXP0	60

HDD1

SATA1RXN	AM10	SATA_RXN1	53
SATA1RXP	AM8	SATA_RXP1	53
SATA1TXN	AP11	SATA_TXN1	53
SATA1TXP	AP10	SATA_TXP1	53

0928 mSATA

SATA2RXN	AD7	SATA_RXN2	60
SATA2RXP	AD5	SATA_RXP2	60
SATA2TXN	AH5	SATA_TXN2	60
SATA2TXP	AH4	SATA_TXP2	60

ODD

SATA3RXN	AB8	SATA_RXN3	60
SATA3RXP	AB10	SATA_RXP3	60
SATA3TXN	AF3	SATA_TXN3	60
SATA3TXP	AF1	SATA_TXP3	60

0928 HDD2

SATA4RXN	V7		
SATA4RXP	Y5		
SATA4TXN	AD3		
SATA4TXP	AD1		
SATA5RXN	Y3		
SATA5RXP	Y1		
SATA5TXN	AB3		
SATA5TXP	AB1		

SATAICOMPO — Y11
SATAICOMPI — Y10 — SATA_COMP R2007 1% 37.4Ohm — +VTT_PCH_VCCIO

SATA3RCOMPO — AB12
SATA3COMPI — AB13 — SATA3_COMP R2047 1% 49.9Ohm — +VTT_PCH_VCCIO

SATA3RBIAS — AH1 — RBIAS_SATA3 R2048 1% 750Ohm — GND

SATALED# — P3 — R2025 @ 10KOhm — +3VS — SATA_LED# — SATA_LED# 66

SATA0GP/GPIO21 — V14 — SATA0GP

SATA1GP/GPIO19 — P1 — BBS_BIT0_R — SP2003 — R0402 — BBS_BIT0 24

SATA

0200-00HU000 C.S 907552 A1 QMVY BGA942 INTEL/COUGAR POINT PCH

HDA_DKEN : Flash Descriptor Security Overide
H = Disabled (Default)
L = Enabled
Note : Rising edge of PWROK

JRST3 1MM_OPEN_M1M2 — HDA_DOCK_EN# — R2008 1KOhm

R1.0 add JRST3 to follow BIC50. Joyoung 0628

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High:Enable

SB_SPKR — R2020 @ 1KOhm — +3VS

ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

ACZ_SDOUT — R2034 @ 1KOhm — +3VSUS_ORG

2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.

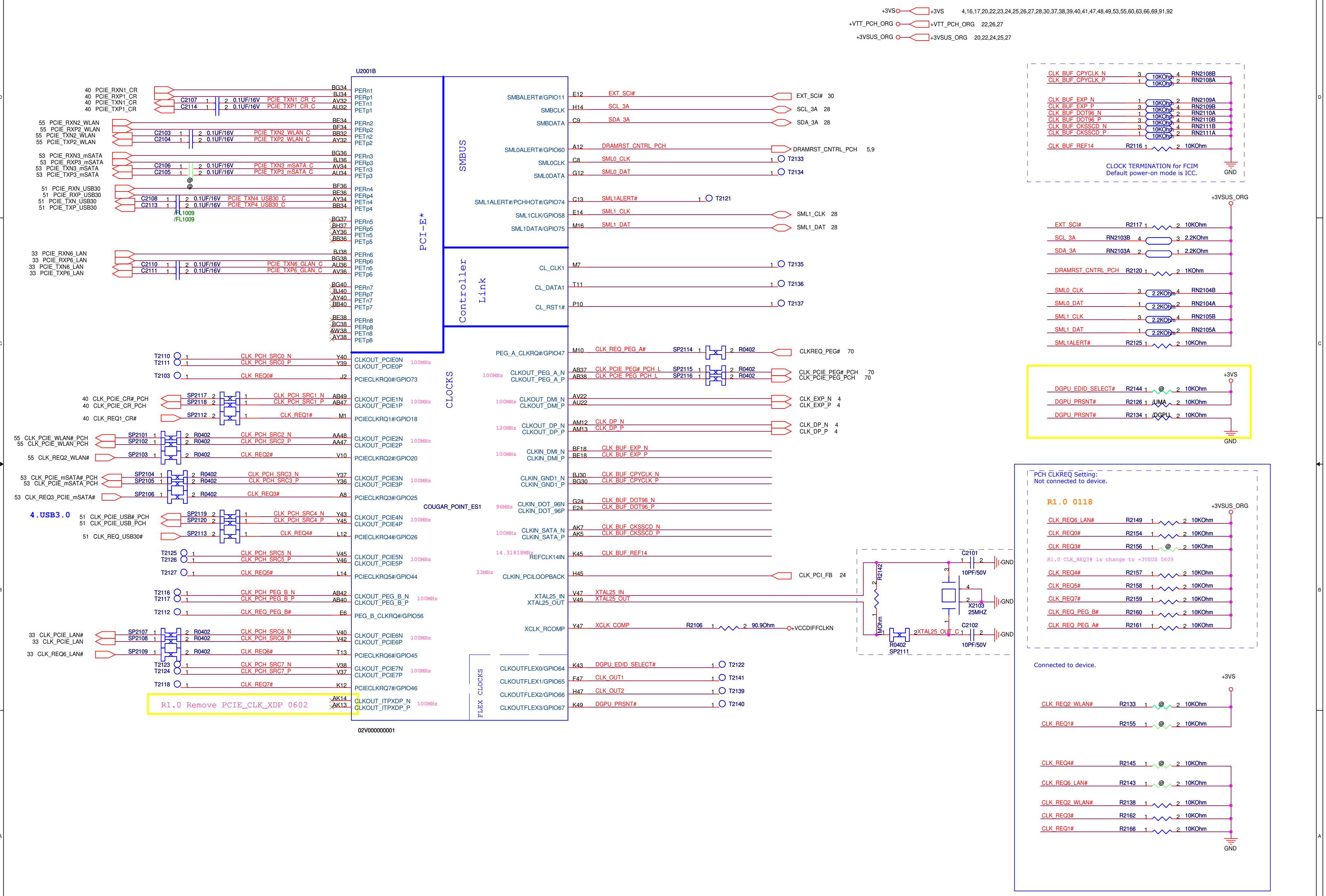
ACZ_SYNC — R2036 1KOhm — +3VSUS_ORG

VCCVRAM use +1.5VS in mobile

ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hrron River Platform Schematic Design Checklist
(438390 page 48)

Pull High — +3VS
INT_SERIRQ — R2026 10KOhm
SATA0GP — R2027 10KOhm

PEGATRON Title : PCH(1)_SATA,IHDA,RTC,LPC
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, February 03, 2012 | Sheet 20 of 94

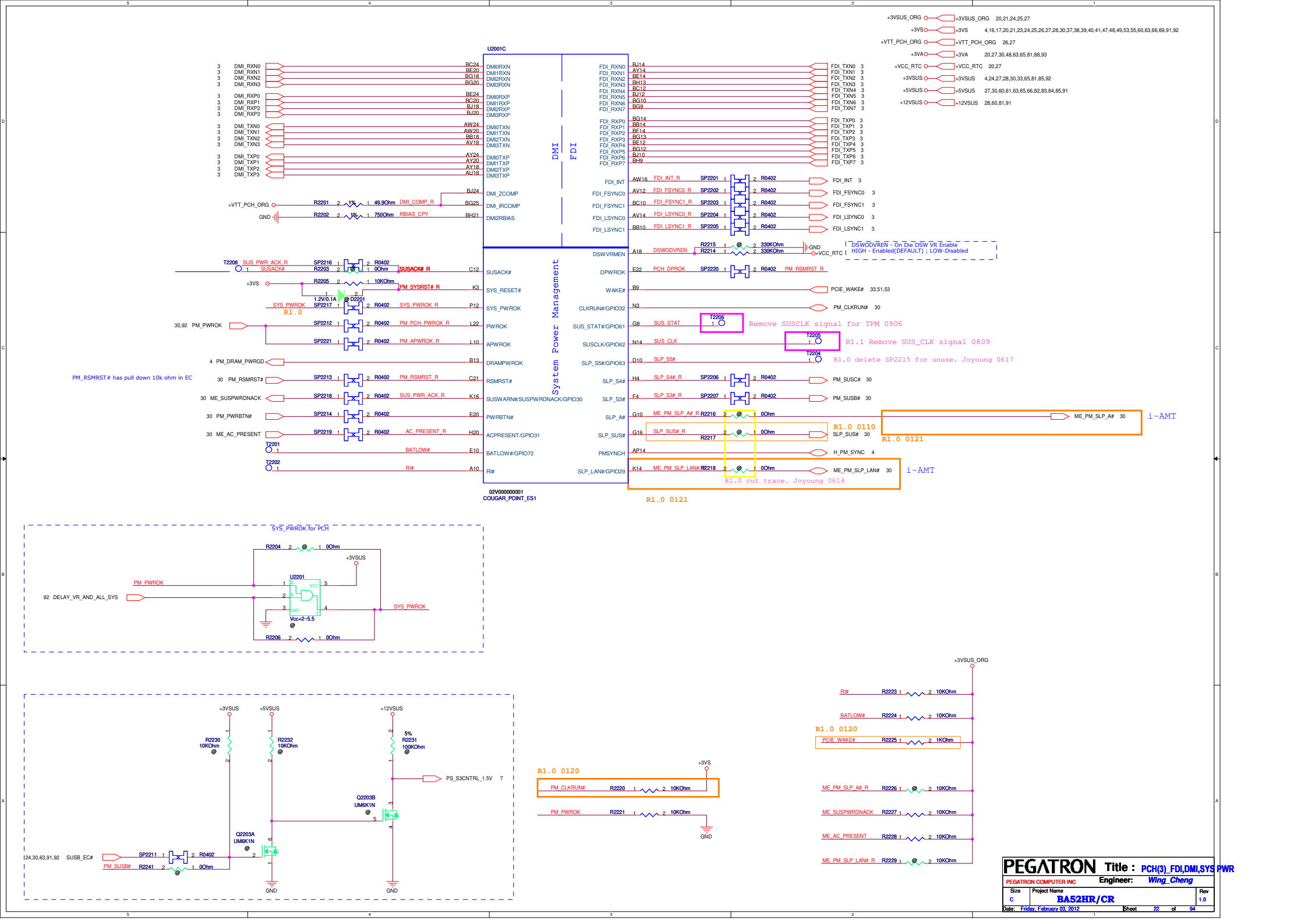


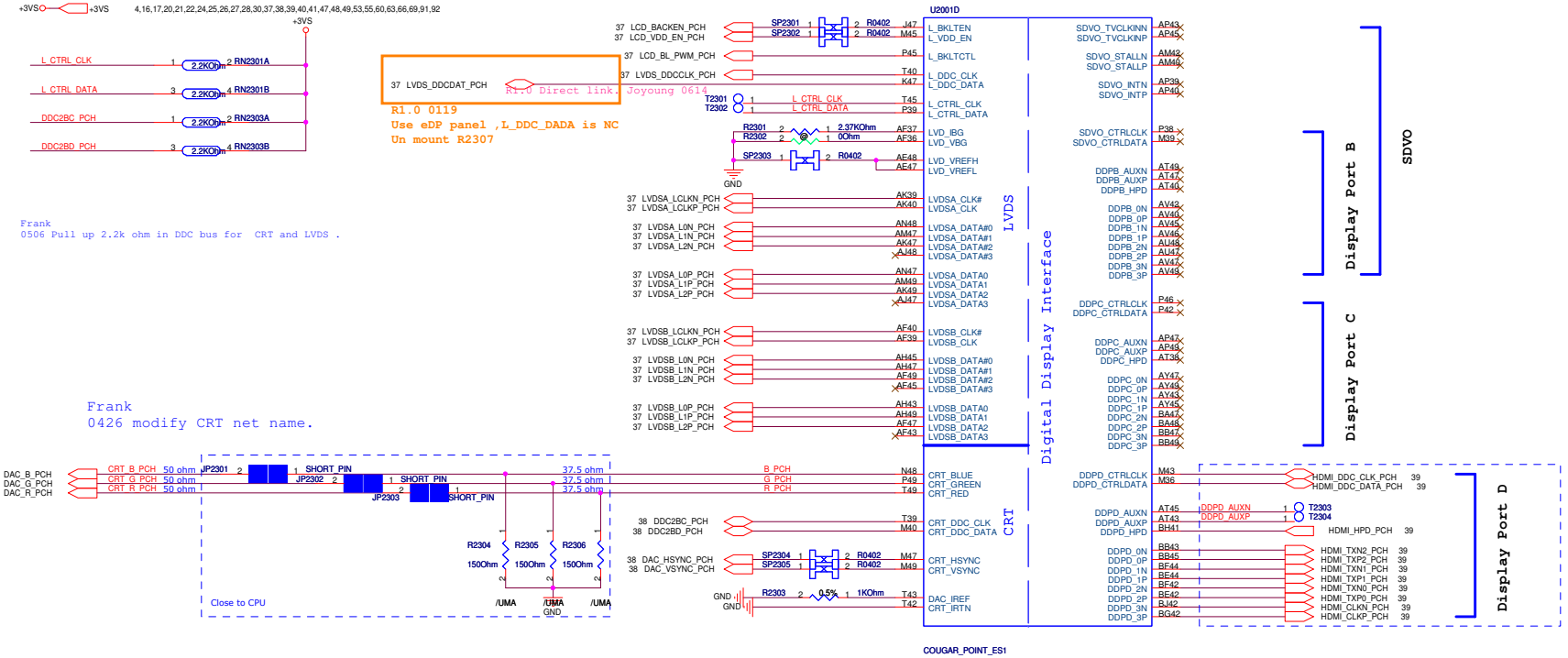
PEGATRON Title : PCH(2)_PCIE,CLK,SMB,PEG

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 21 of 94


U2001C
DMI
FDI
System Power Management
02V000000001
COUGAR_POINT_ES1
SYS_PWROK for PCH
U2201
Vcc=2-5.5
R1.0 0120
R1.0 0121
R1.0 0110
R1.1 Remove SUS_CLK signal 0809
R1.0 delete SP2215 for unuse. Joyoung 0617
R1.0 cut trace. Joyoung 0614
Remove SUSCLK signal for TPM 0906
DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW-Disabled
PM_RSMRST# has pull down 10k ohm in EC
i-AMT
i-AMT
PEGATRON
PEGATRON COMPUTER INC
Title : PCH(3)_FDI,DMI,SYS PWR
Engineer: Wing_Cheng
Size C
Project Name BA52HR/CR
Rev 1.0
Date: Friday, February 03, 2012
Sheet 22 of 94



CRT Disable: (For discrete graphic)

1. NC:

CRT_RED,CRT_GREEN,CRT_BLUE

CRT_HSYCN,CRT_VSYNC

2. 1-kΩ ±0.5% pull-down to GND:

DAC_IREF

3. Connected to GND:

CRT_ITRN

4. Connect to +V3.3:

VCCADAC

DisPlay Port Disable: (For discrete graphic)

1. NC:

ALL

LVDS Disable: (For discrete graphic)

1. NC:

LVDSA_DATA [3:0], LVDSA_DATA# [3:0],

LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],

LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#

L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH

LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:

VccALVDS,VccTX_LVDS

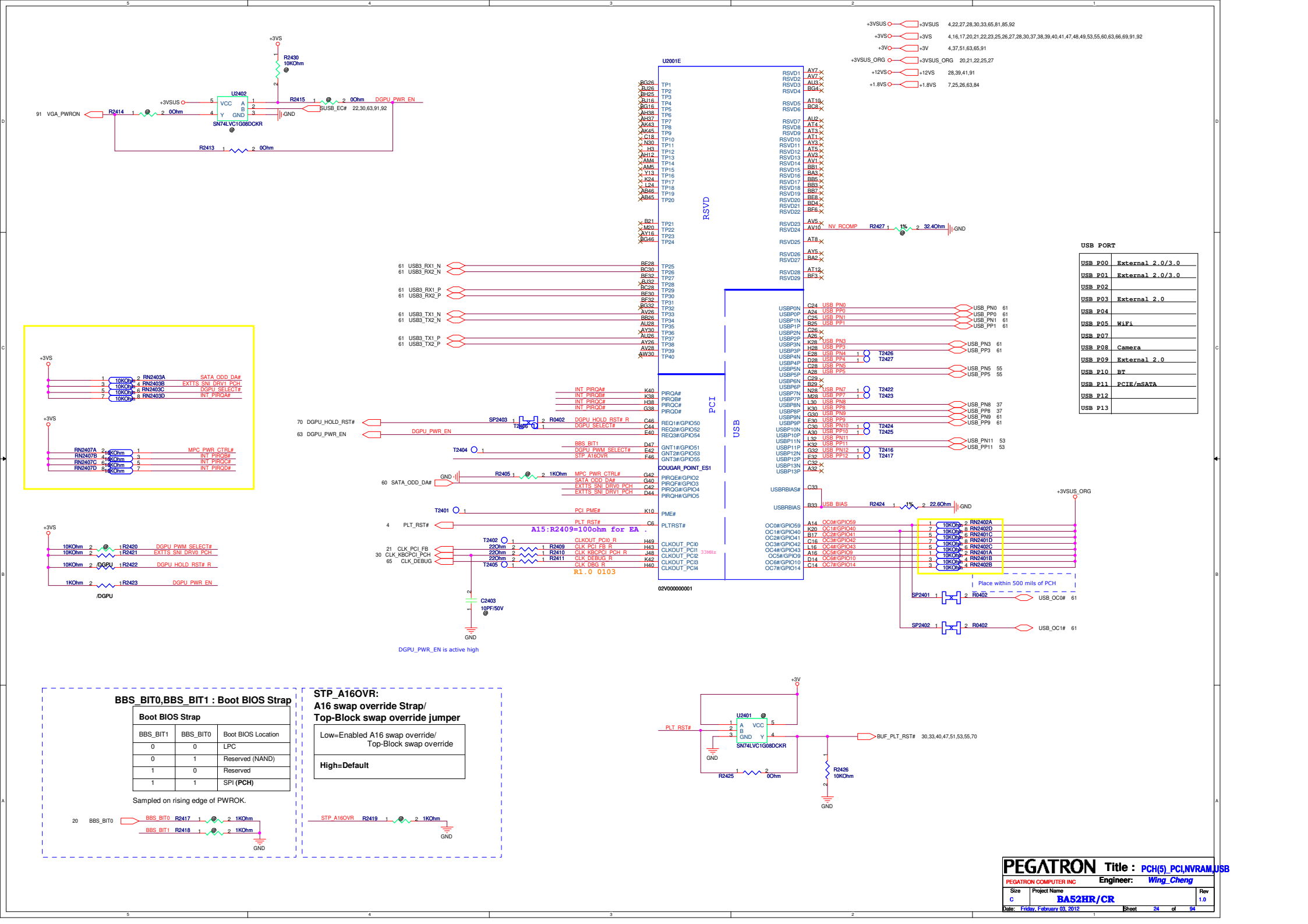
PEGATRON COMPUTER INC

Title : PCH(4)_DP,LVDS,CRT

Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 23 of 94


+3VSUS 4,22,27,28,30,33,65,81,85,92
+3VS 4,16,17,20,21,22,23,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92
+3V 4,37,51,63,65,91
+3VSUS_ORG 20,21,22,25,27
+12VS 28,39,41,91
+1.8VS 7,25,26,63,84
U2001E
RSVD
PCI
USB
COUGAR_POINT_ES1
02V000000001
R2427 1% 32.4Ohm
NV_RCOMP
USB PORT
USB P00 External 2.0/3.0
USB P01 External 2.0/3.0
USB P02
USB P03 External 2.0
USB P04
USB P05 WiFi
USB P07
USB P08 Camera
USB P09 External 2.0
USB P10 BT
USB P11 PCIE/mSATA
USB P12
USB P13
U2402
SN74LVC1G08DCKR
R2414 0Ohm
R2415 0Ohm
R2413 0Ohm
DGPU_PWR_EN
VGA_PWRON
SUSB_EC#
R2430 10KOhm
SP2403
R0402
DGPU_HOLD_RST# R
DGPU_SELECT#
DGPU_PWR_EN
BBS_BIT1
DGPU_PWM_SELECT#
STP_A16OVR
T2404
T2405
T2406
R2405 1KOhm
MPC_PWR_CTRL#
SATA_ODD_DA#
EXTTS_SNI_DRV0_PCH
EXTTS_SNI_DRV1_PCH
PCI_PME#
PLT_RST#
A15:R2409=100ohm for EA .
R1.0 0103
CLK_PCI_FB_R
CLK_KBCPCI_PCH_R
CLK_DEBUG_R
CLK_DBG_R
33MHz
C2403 10PF/50V
DGPU_PWR_EN is active high
R2424 1% 22.6Ohm
USB_BIAS
+3VSUS_ORG
Place within 500 mils of PCH
SP2401
SP2402
R0402
USB_OC0#
USB_OC1#
U2401
SN74LVC1G08DCKR
BUF_PLT_RST#
R2425 0Ohm
R2426 10KOhm
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap
Boot BIOS Strap
BBS_BIT1 BBS_BIT0 Boot BIOS Location
0 0 LPC
0 1 Reserved (NAND)
1 0 Reserved
1 1 SPI (PCH)
Sampled on rising edge of PWROK.
R2417 1KOhm
R2418 1KOhm
STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper
Low=Enabled A16 swap override/
Top-Block swap override
High=Default
R2419 1KOhm
PEGATRON
Title : PCH(5)_PCI,NVRAM,USB
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size C
Project Name BA52HR/CR
Rev 1.0
Date: Friday, February 03, 2012
Sheet 24 of 94

	PCB_ID1	PCB_ID0
A	L	L
B	L	H
C	H	L
MP		

R1.0

Add PCH_GPIO0_R.

Delete ICC_EN#.

Add PM_LANPHY_EN

Add HOST_ALERT#1_R.

Add SATA_DET#4_R.

DGPU_PWROK has 100 ms software delay , no hardware delay requirement

Reserve PCH_GPIO24

Add PLL_ODVR_EN.

Add PSATA_PWR_EN#1_R.

Add SATA_ODD_PRSNT#_R and FDI_OVRVLTG.

Add CRIT_TEMP_REP#_R.

+3VS 4,16,17,20,21,22,23,24,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92

+3VSUS 4,22,24,27,28,30,33,65,81,85,92

+3VSUS_ORG 20,21,22,24,27

R2525 10KOhm PCB_ID0

R2527 10KOhm PCB_ID1

R2526 10KOhm

R2528 10KOhm

GND GND

Frank
0502 Modify PCB_ID

U2001F

GPIO / CPU/MISC

69 GSENSOR_INT1_PCH	R2501 100Ohm	PCH_GPIO0_R	T7 BMBUSY#/GPIO0
		GPIO1	A42 TACH1/GPIO1
	T2503	DGPU_HPD_INTR#	H36 TACH2/GPIO6
37 eDP_ON#	eDP_ON#		E38 TACH3/GPIO7
51 USB30_EXT_SMI#		USB30_EXT_SMI#	C10 GPIO8
53,55 WLAN_RST#_PCH	SP2502 R0402	PM_LANPHY_EN	C4 LAN_PHY_PWR_CTRL/GPIO12
30,65 EXT_SMI#	SP2501 R0402	HOST_ALERT#1_R	G2 GPIO15
		SATA_DET#4	U2 SATA4GP/GPIO16
87,91,92 DGPU_PWROK	DGPU_PWROK		D40 TACH0/GPIO17
66 WLAN_LED		WLAN_LED	T5 SCLOCK/GPIO22
T2509 LAN_LPWR	SP2504 R0402	PCH_GPIO24	E8 GPIO24/MEM_LED
		GPIO27	E16 GPIO27
		WLAN_ON_R	P8 GPIO28
		STP_PCI#	K1 STP_PCI#/GPIO34
T2510		SATA_PWR_EN#1_R	K4 GPIO35
60 SATA_ODD_PRSNT#	SP2503 R0402	SATA_ODD_PRSNT#_R	V8 SATA2GP/GPIO36
		FDI_OVRVLTG	M5 SATA3GP/GPIO37
		PCB_ID0	N2 SLOAD/GPIO38
		PCB_ID1	M3 SDATAOUT0/GPIO39
55 BT_ON_PCH			V13 SDATAOUT1/GPIO48
30 PCH_ALERT#	SP2505 R0402	CRIT_TEMP_REP#_R	V3 SATA5GP/GPIO49
T2508		BT_LED	D6 GPIO57

TACH4/GPIO68	C40	SATA_ODD_PWRGT 60
TACH5/GPIO69	B41 R2511 1% 1.5KOhm	GND
TACH6/GPIO70	C41 R2512 1% 1.5KOhm	+3VS
TACH7/GPIO71	A40 R2513 1% 1.5KOhm	+3VS
A20GATE	P4	A20GATE 30
PECI	AU16 H_PECI_R 0Ohm R2514 43Ohm R2515	H_PECI 4, H_PECI_EC 30
RCIN#	P5	RCIN# 30
PROCPWRGD	AY11	H_CPUPWRGD 4
THRMTRIP#	AY10 PM_THRMTRIP# 390Ohm 1% R2516 R2517 56Ohm	H_THRMTRIP# 4,47 +VCCP
INIT3_3V#	T14 INIT3_3V# T2504	
DF_TVS	AY1 NV_CLE R2502 1KOhm R2503 2.2KOhm	H_SNB_IVB# 4 +1.8VS
TS_VSS1	AH8	
TS_VSS2	AK11	
TS_VSS3	AH10	
TS_VSS4	AK10	GND
NC_1	P37	

need close to EC

TS Signal Disable Guideline
TS_VSS[1:4] should pull down to GND
Design Guide 0.9 (436735)

NCTF

A4	Vss_NCTF1	Vss_NCTF15	BG2
A44	Vss_NCTF2	Vss_NCTF16	BG48
A45	Vss_NCTF3	Vss_NCTF17	BH3
A46	Vss_NCTF4	Vss_NCTF18	BH47
A5	Vss_NCTF5	Vss_NCTF19	BJ4
A6	Vss_NCTF6	Vss_NCTF20	BJ44
B3	Vss_NCTF7	Vss_NCTF21	BJ45
B47	Vss_NCTF8	Vss_NCTF22	BJ46
BD1	Vss_NCTF9	Vss_NCTF23	BJ5
BD49	Vss_NCTF10	Vss_NCTF24	BJ6
BE1	Vss_NCTF11	Vss_NCTF25	C2
BE49	Vss_NCTF12	Vss_NCTF26	C48
BF1	Vss_NCTF13	Vss_NCTF27	D1
BF49	Vss_NCTF14	Vss_NCTF28	D49
		Vss_NCTF29	E1
		Vss_NCTF30	E49
		Vss_NCTF31	F1
		Vss_NCTF32	F49

COUGAR_POINT_ES1 02V000000001

+3VSUS_ORG

R1.0 0126 Intel Comments

EXT_SMI# R2529 1KOhm

USB30_EXT_SMI# R2531 10KOhm

PM_LANPHY_EN R2538 /pIAMT 10KOhm

PCH_GPIO24 R2541 10KOhm

R1.0 0120

R1.0 mount R2541 for LAN_LPWR 0615

RCIN# has pull high at EC side

DGPU_HPD_INTR# R2534 10KOhm

PCH_ALERT# R2535 10KOhm

R1.0 0119

DGPU_PWROK R2539 10KOhm

eDP_ON# R2547 10KOhm

Unused GPIO

GSENSOR_INT1_PCH R2536 10KOhm

GPIO1 R2545 @ 10KOhm

R1.0 0119

STP_PCI# R2537 10KOhm

SATA_DET#4 R2546 10KOhm

GPIO27 R2548 10KOhm

#438390 Checklist

GND

R1.0 REMOVE DGPU_PWROK schematic 0602

DGPU_PWROK R2540 @ 10KOhm

GND

+3VS +3VS

R2549 10KOhm

R2550 10KOhm

53,55 WLAN_ON

Q2501B UM6K1N

Q2501A UM6K1N

WLAN_ON_R

GND GND

+3VS R2518 1% 1KOhm FDI_OVRVLTG R2519 100KOhm GND

FDI TERMINATION VOLTAGE OVERRIDE
- GPIO37 (FDI_OVRVLTG)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT

+3VS R2520 1% 200KOhm SATA_ODD_PRSNT#_R

DMI TERMINATION VOLTAGE OVERRIDE
- GPIO36 (SATA_ODD_PRSNT#)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT

WLAN_ON_R R2521 @ 1KOhm GND

PLL ON DIE VR ENABLE
HIGH - DISABLED (DEFAULT)
LOW - ENABLED

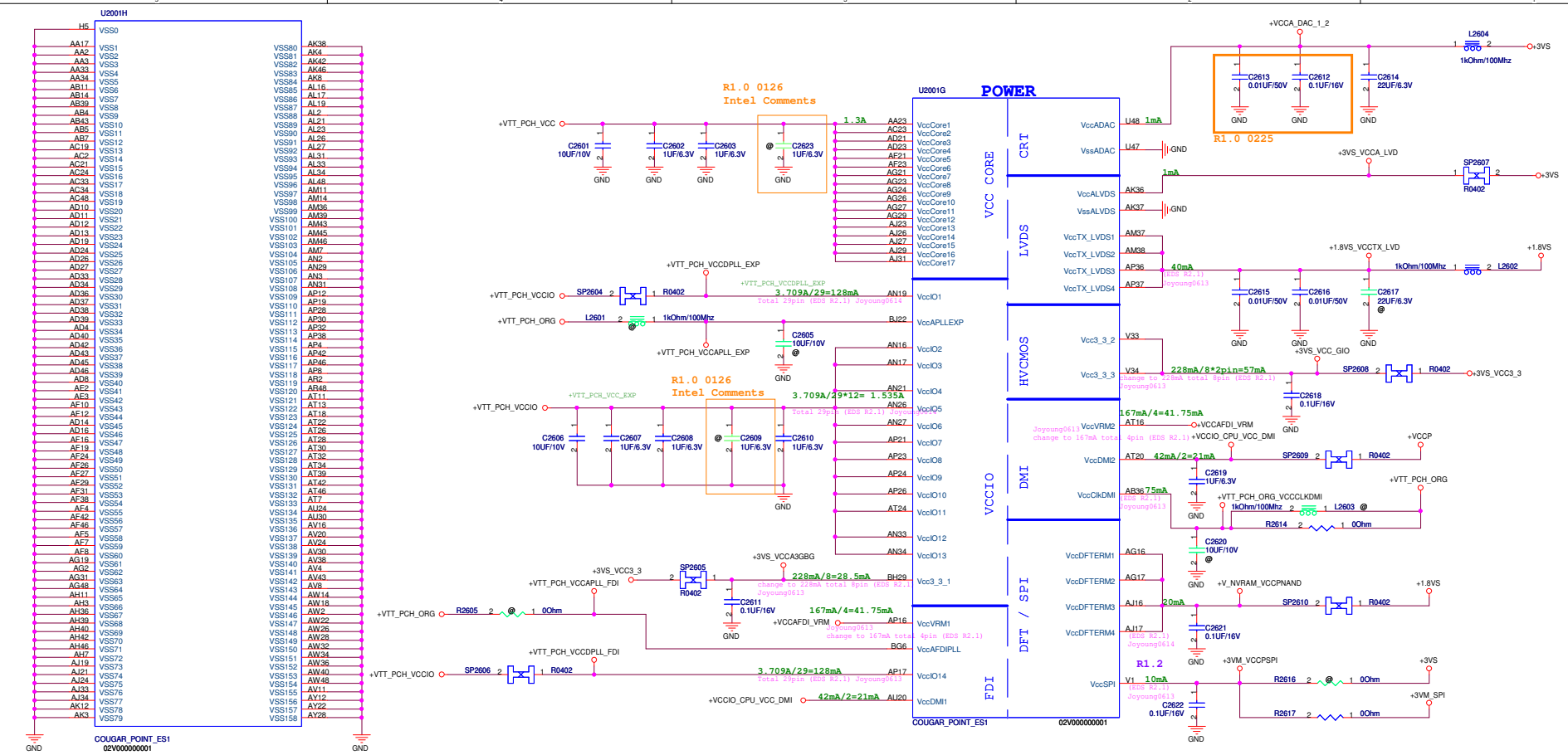
R1.0 Change net name for single net. Joyoung 0621

PEGATRON Title : PCH(6)_CPU,GPIO,MISC

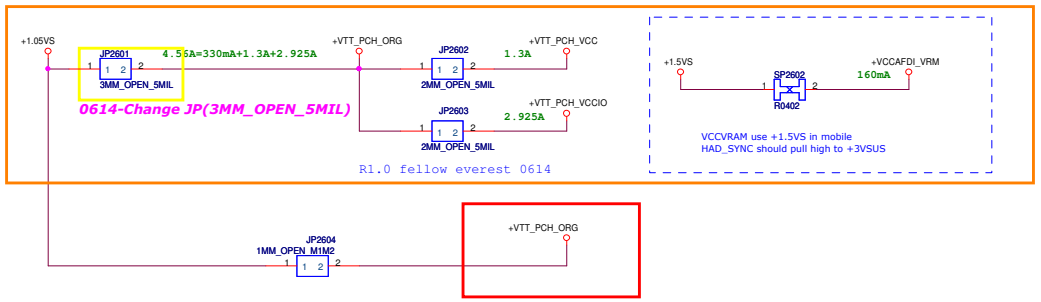
PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 25 of 94



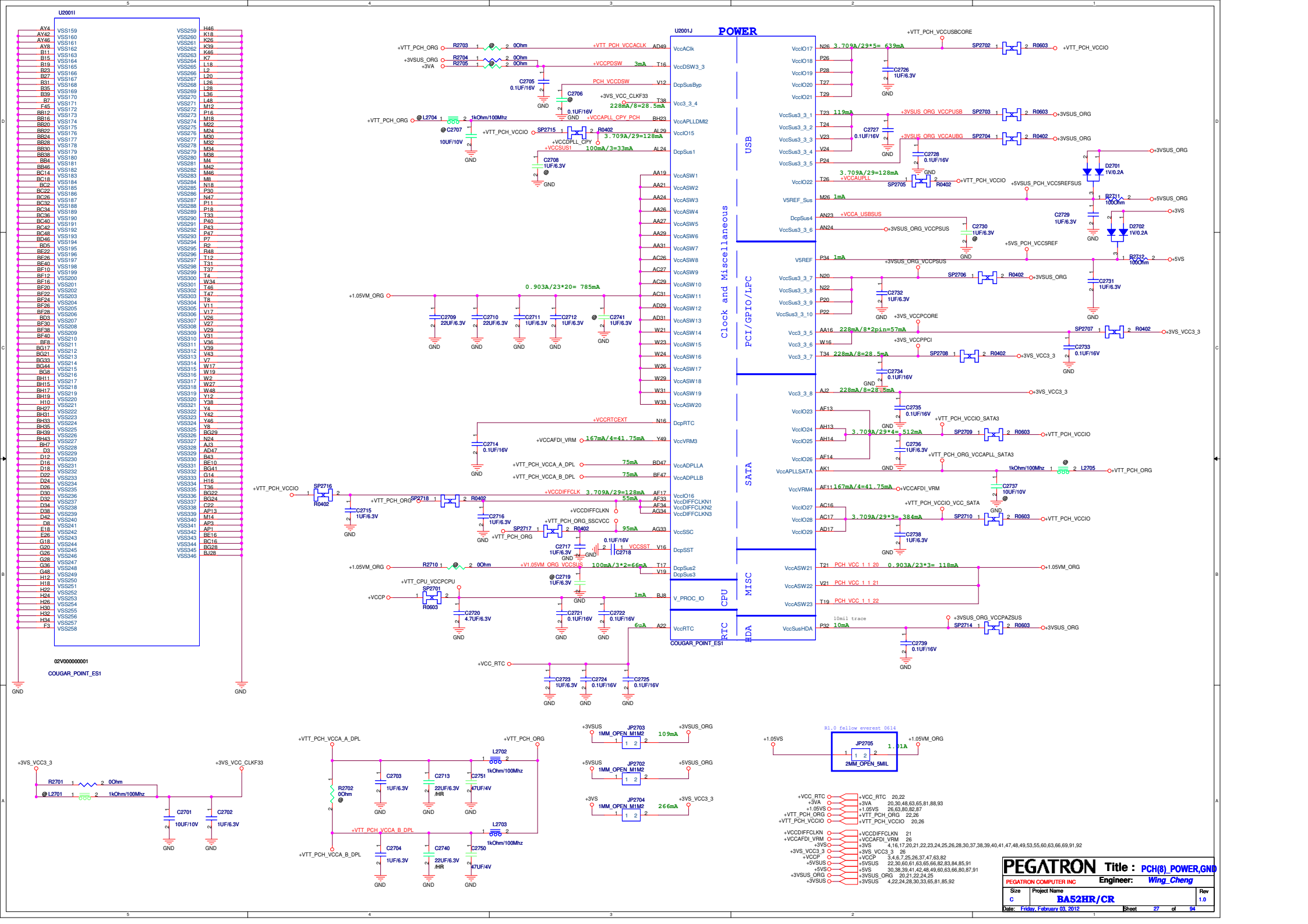
R1.0 0118



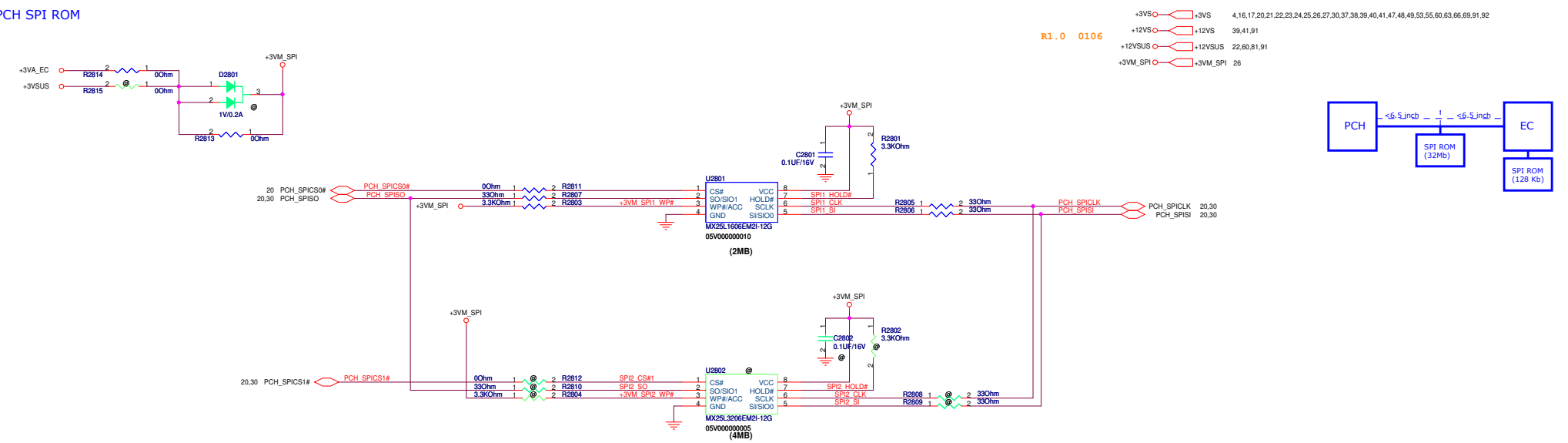
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	20,27
+VTT_PCH_ORG	+VTT_PCH_ORG	22,27
+1.05VS	+1.05VS	27,63,80,82,87
+1.5VS	+1.5VS	53,55,63,91
+VCCAFDI_VRM	+VCCAFDI_VRM	27
+3VS	+3VS	4,16,17,20,21,22,23,24,25,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92
+3VS_VCC3_3	+3VS_VCC3_3	27
+3VM_SPI	+3VM_SPI	28
+1.8VS	+1.8VS	7,25,63,84
+VCCP	+VCCP	3,4,6,7,25,27,37,47,63,82

R1.0
Delete
+VTT_PCH_VCC
+VTT_PCH_VCCDPLL_EXP
+VTT_PCH_VCCAPLL_EXP
+VTT_PCH_VCCDPLL_FDI
+VTT_PCH_VCCAPLL_FDI
+3VS_VCCA3GBG
+3VS_VCC_GIO
+VCCA_DAC_1_2
+3VS_VCCA_LVDS
+3VM_VCCPSPI
+V_NVRAM_VCCPNAND
+1.8VS_VCCTX_LVD
+VCCIO_CPU_VCC_DMI
+VTT_PCH_ORG_VCCCLKDMI

PEGATRON	Title :	PCH(7)_POWER,GND		
PEGATRON COMPUTER INC	Engineer:	Wing_Cheng		
Size: C	Project Name: BA52HR/CR		Rev: 1.0	
Date: Friday, February 03, 2012	Sheet: 26	of: 94		

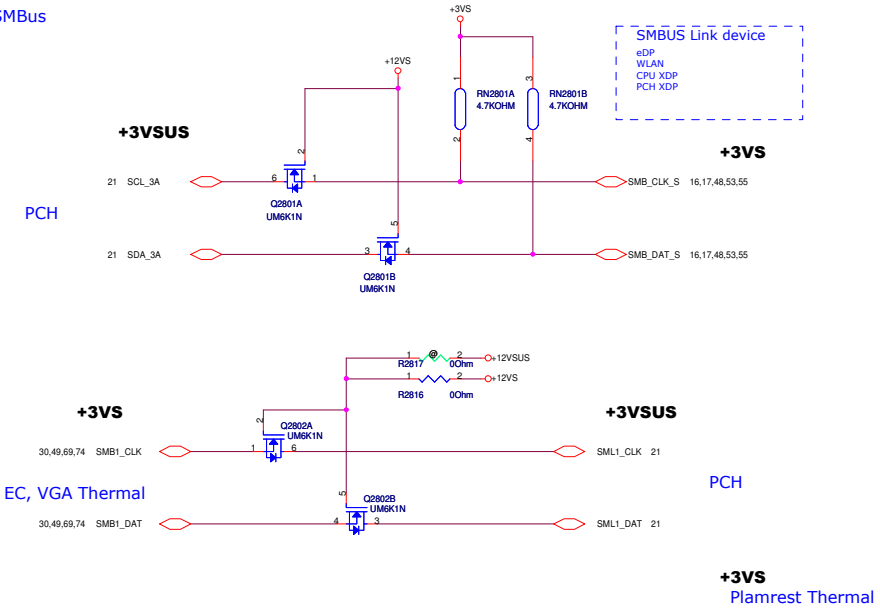

POWER
U2001I
U2001J
COUGAR_POINT_ES1
02V000000001
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA
+VTT_PCH_VCCUSBCORE
+VTT_PCH_VCCIO
+3VSUS_ORG
+5VSUS_ORG
+3VS
+5VS
+VTT_PCH_ORG
+VCCACLK
+VCCPDSW
+3VS_VCC_CLKF33
+VCCAPLL_CPY_PCH
+VCCDPLL_CPY
+VCCSUS1
+VCCAUPLL
+VCCA_USBSUS
+3VSUS_ORG_VCCPSUS
+5VS_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+3VS_VCCPCORE
+3VS_VCCPPCI
+3VS_VCC3_3
+VCCRTCEXT
+VCCADFDI_VRM
+VTT_PCH_VCCA_A_DPL
+VTT_PCH_VCCA_B_DPL
+VCCDIFFCLK
+VCCDIFFCLKN
+VTT_PCH_ORG_SSCVCC
+1.05VM_ORG
+V1.05VM_ORG_VCCSUS
+VTT_CPU_VCCPCPU
+VCCP
+VTT_PCH_VCCIO_SATA3
+VTT_PCH_ORG_VCCAPLL_SATA3
+VTT_PCH_VCCIO_VCC_SATA
+3VSUS_ORG_VCCPAZSUS
+VCC_RTC
+3VSUS_ORG_VCCPUSB
+3VSUS_ORG_VCCAUBG
PCH_VCCDSW
+VCCDIFFCLKN
+VCCADFDI_VRM
+VTT_PCH_VCCA_A_DPL
+VTT_PCH_VCCA_B_DPL
+VTT_PCH_ORG
+3VS_VCC3_3
+3VS_VCC_CLKF33
+1.05VS
+1.05VM_ORG
+5VSUS
+3VSUS_ORG
+3VS
+3VS_VCC3_3
+VCC_RTC
+3VA
+1.05VS
+VTT_PCH_ORG
+VTT_PCH_VCCIO
+VCCDIFFCLKN
+VCCADFDI_VRM
+3VS
+3VS_VCC3_3
+VCCP
+5VSUS
+5VS
+3VSUS_ORG
+3VSUS
PEGATRON
Title : PCH(8)_POWER,GND
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size C
Project Name BA52HR/CR
Rev 1.0
Date: Friday, February 03, 2012
Sheet 27 of 94

PCH SPI ROM



SPI Debug Connector

PCH SMBus



PEGATRON Title : PCH(9)_SPI,SMB

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 28 of 94

PEGATRON Title : CLK_ICS9LRS3197

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 29 of 94

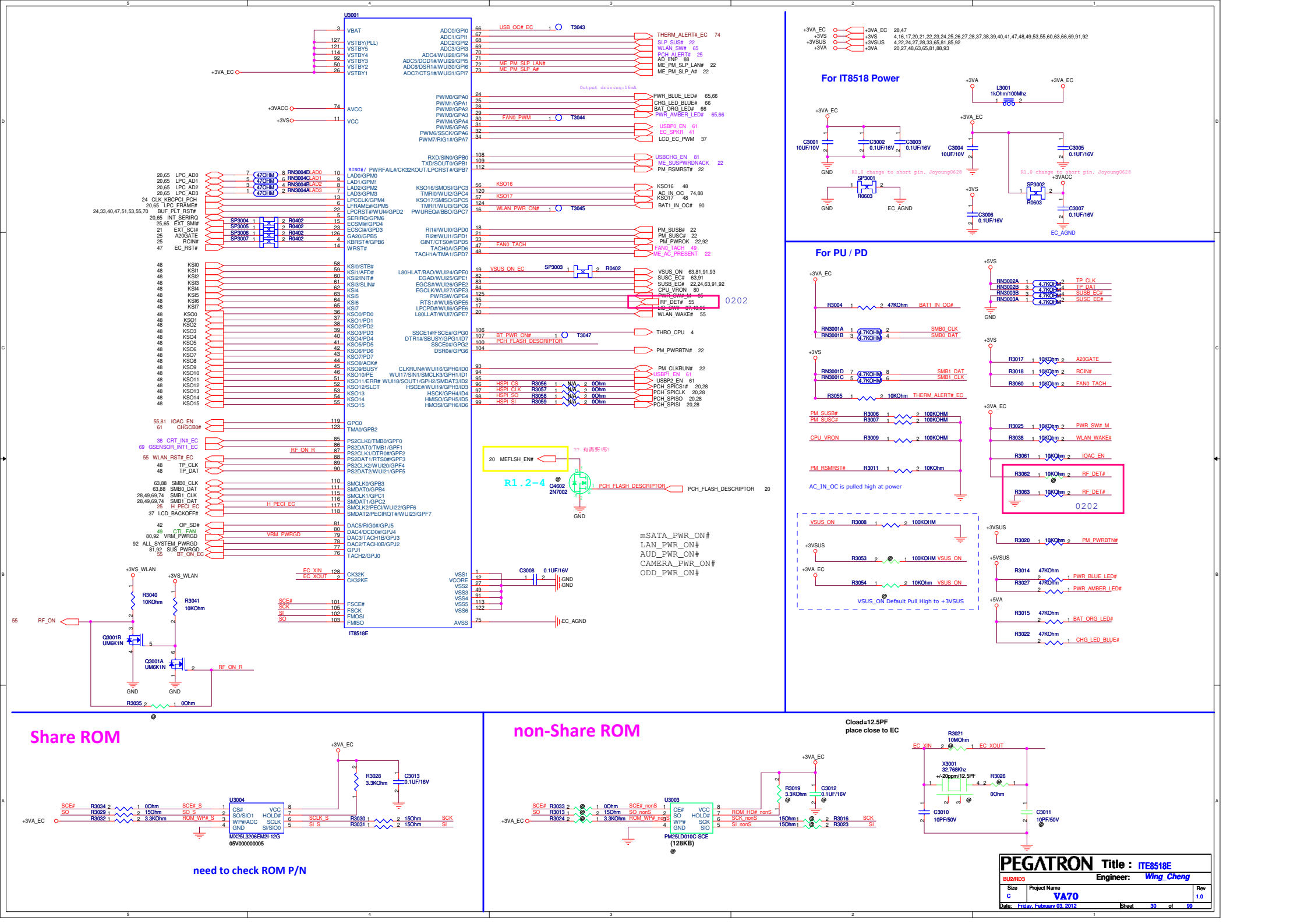
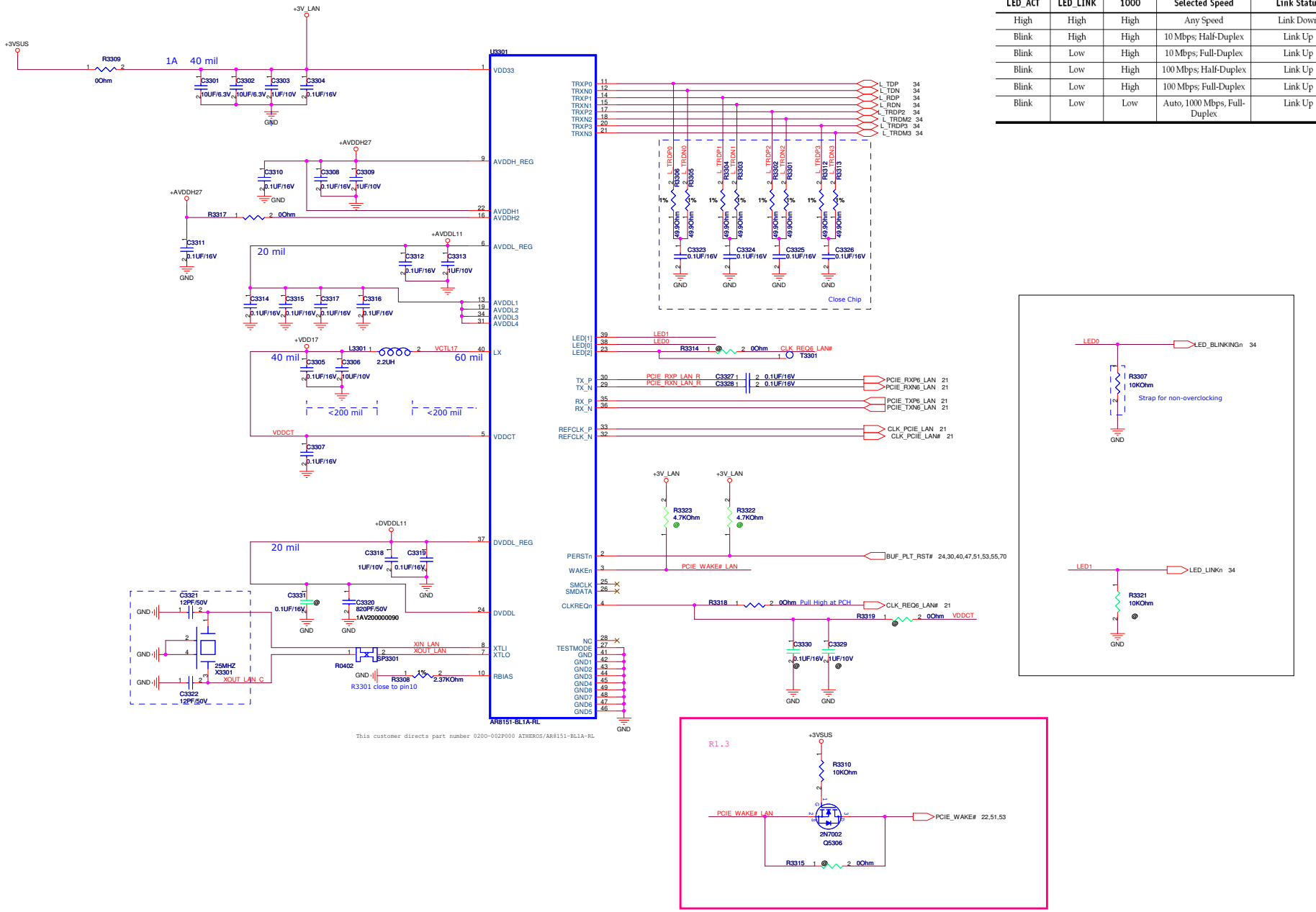

U3001
IT8518E
For IT8518 Power
For PU / PD
Share ROM
non-Share ROM
need to check ROM P/N
Cload=12.5PF
place close to EC
mSATA_PWR_ON#
LAN_PWR_ON#
AUD_PWR_ON#
CAMERA_PWR_ON#
ODD_PWR_ON#
AC_IN_OC is pulled high at power
VSUS_ON Default Pull High to +3VSUS
PEGATRON
Title : ITE8518E
Engineer: Wing_Cheng
BU2/RD3
Size C
Project Name VA70
Rev 1.0
Date: Friday, February 03, 2012
Sheet 30 of 99

Table 2-6. **LED Link Table**

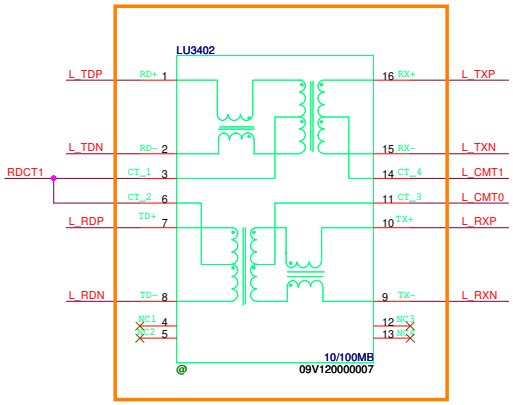
LED[0] LED_ACT	LED[1] LED_LINK	LED[2] LED_LINK_ 1000	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Blink	High	High	10 Mbps; Half-Duplex	Link Up
Blink	Low	High	10 Mbps; Full-Duplex	Link Up
Blink	Low	High	100 Mbps; Half-Duplex	Link Up
Blink	Low	High	100 Mbps; Full-Duplex	Link Up
Blink	Low	Low	Auto, 1000 Mbps, Full-Duplex	Link Up



This customer directs part number 0200-002P000 ATHEROS/AR8151-BL1A-RL

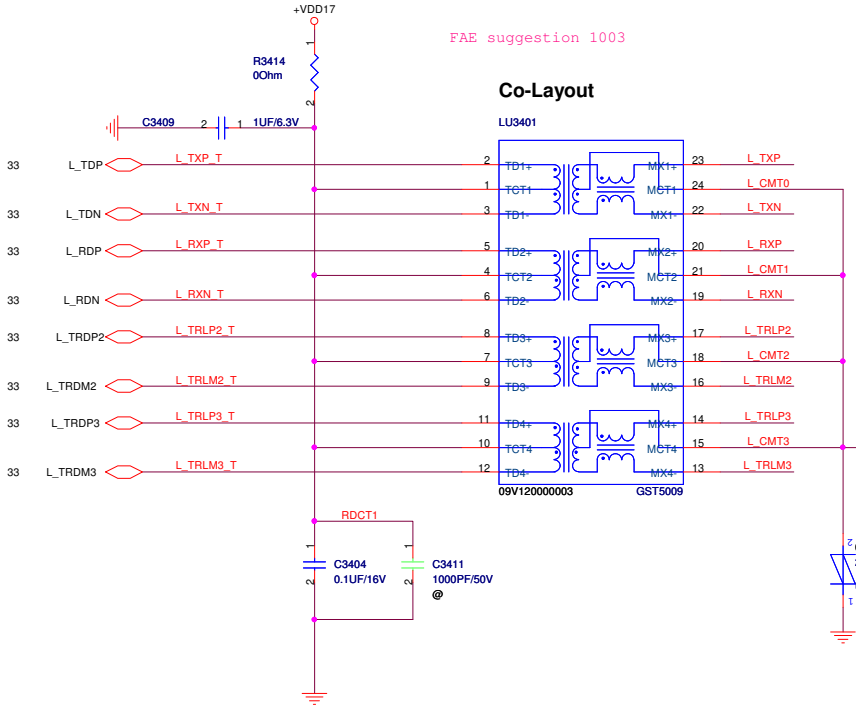
PEGATRON	Title : LAN_AR8151L			
BG1-CSC-HW R&D Dept.5	Engineer: Ahren_chen			
Size: Custom	Project Name: T13M_RG			Rev: 1.0
Date: Friday, February 03, 2012	Sheet 33 of 99			

11/30 Swap for LU3401/LU3402 co-lay(Elmer)

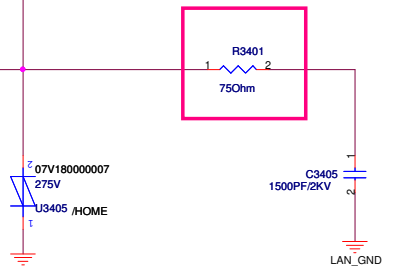


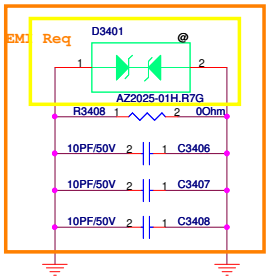
FAE suggestion 1003

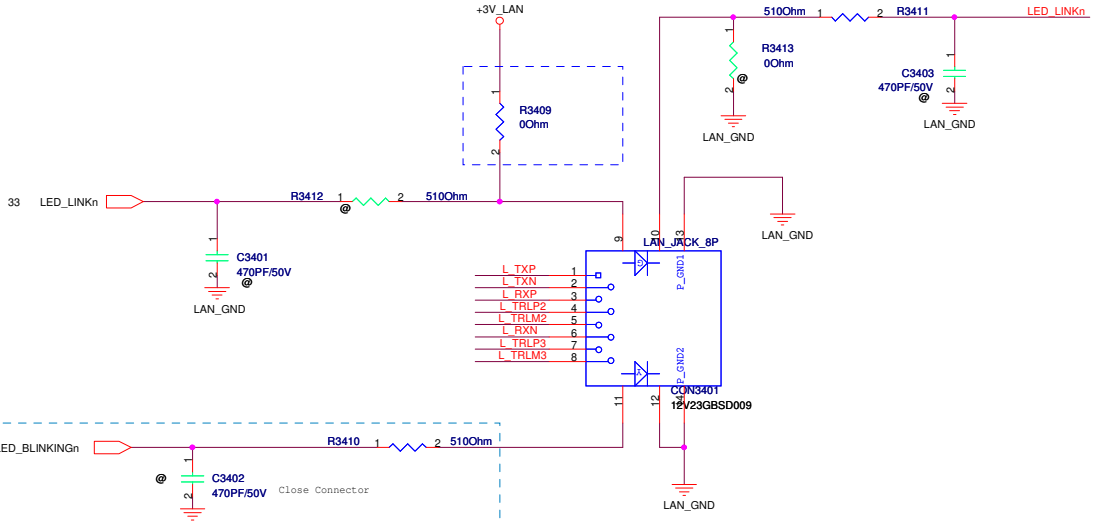
Co-Layout

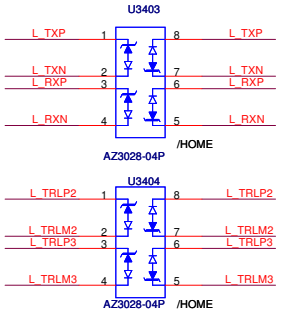


EMI suggest to change 0805 size 0921









<variant_name>

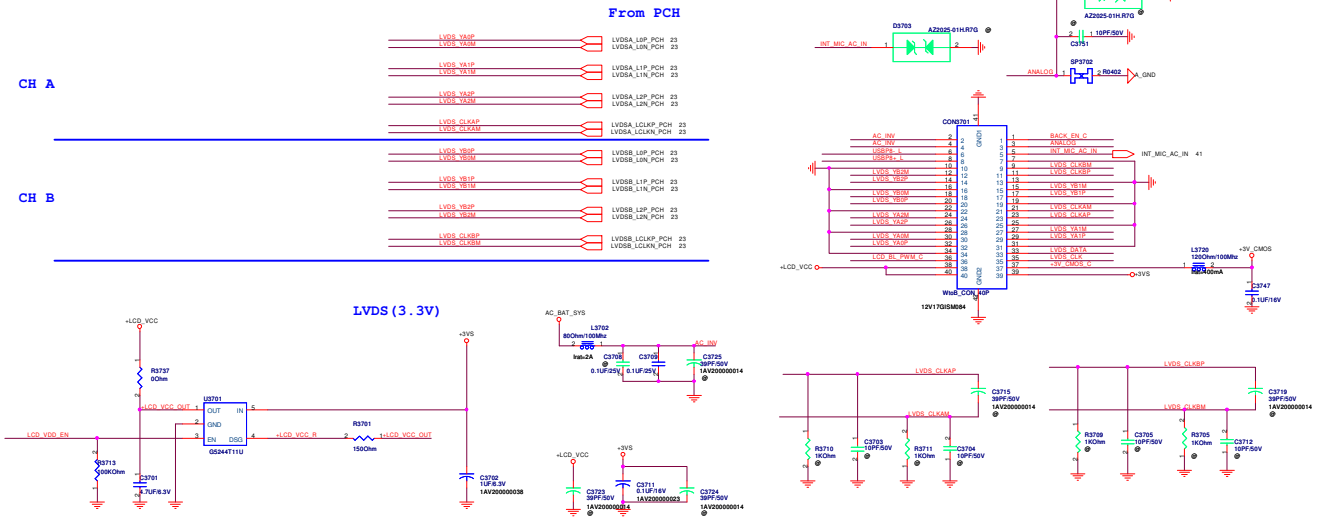
PEGATRON Title : RJ45/ RJ11

BG1-CSC-HW R&D Dept.5 Engineer: Ahren_chen

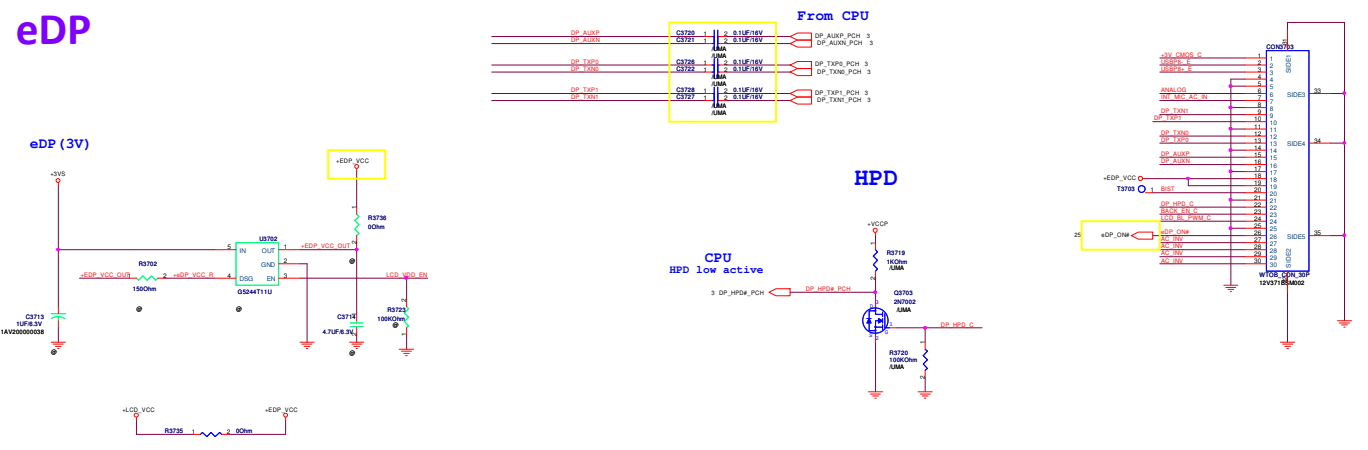
Size	Project Name	Rev
Custom	PLFG	1.0

Date: Friday, February 03, 2012 Sheet 34 of 99

LVDS



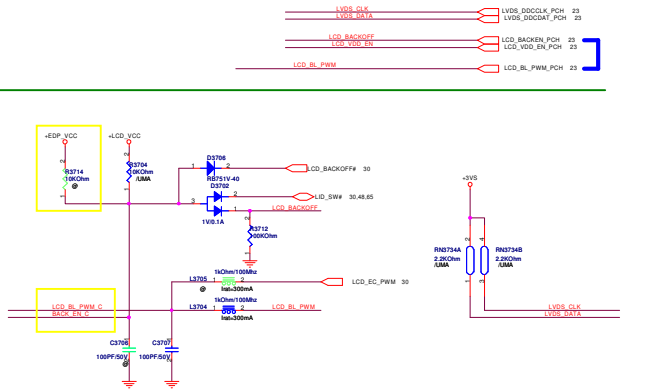
eDP



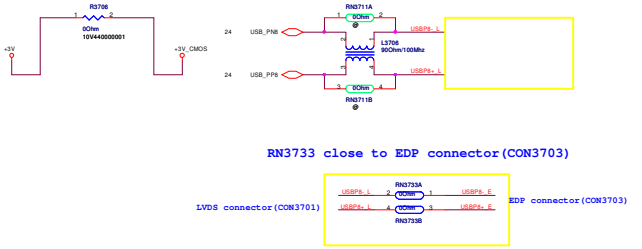
LVDS/eDP control signal

LVDS/EDP共用pin

LVDS/EDP共用pin



USB Camera



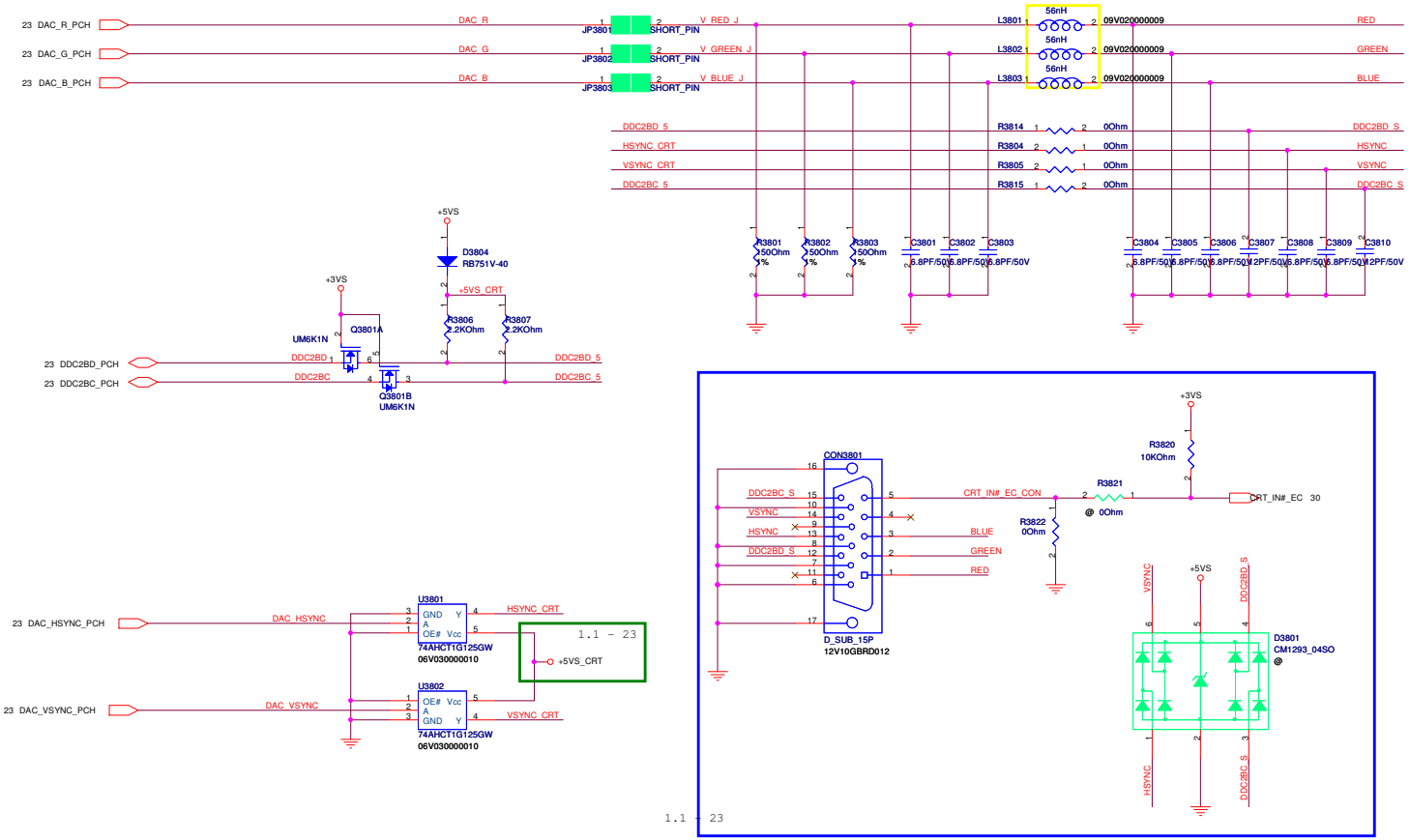
PEGATRON Title : LVDS CONN

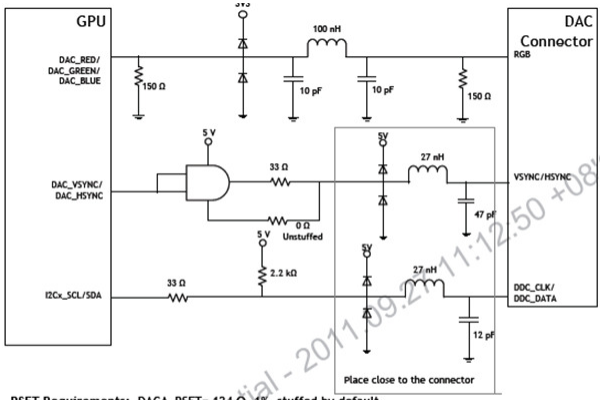
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, February 08, 2019 Sheet 37 of 58

Check UMA and DSC inductor value



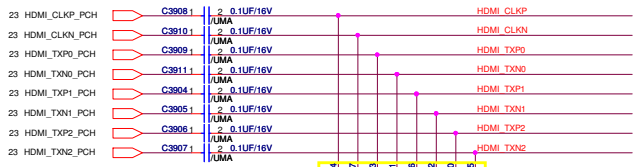


RSET Requirements: DACA_RSET= 124 Ω, 1%, stuffed by default.

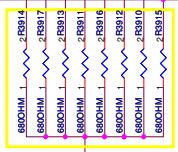
Figure 71. GPU-DAC Connections

The LC filter circuit(NV DSC only)
DDC:L=27nH,C=12PF
HSYNC/VSYNC:L=27nH,C=47PF
RGB:L=100nH,C=10PF

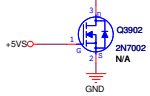
PEGATRON	Title : CRT		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size: Custom	Project Name: BA52HR/CR		Rev: 1.0
Date: Friday, February 03, 2012	Sheet 38 of 77		



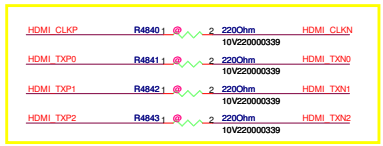
Close to connector and do T routing

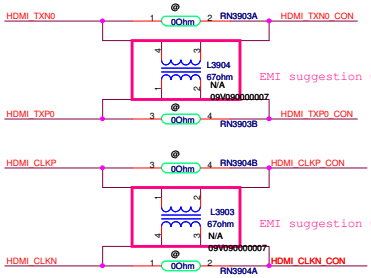


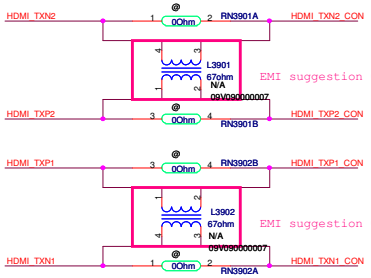
R3910,R3911,R3912,R3913,R3914,R3915,R3916,R3917
Intel design guide : 680ohm /UMA
NV reference schematics : 499ohm /DGPUO



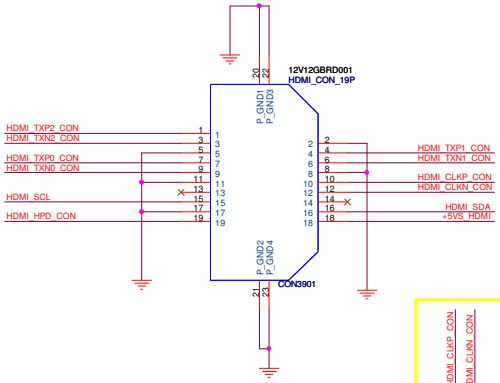
EMI solution

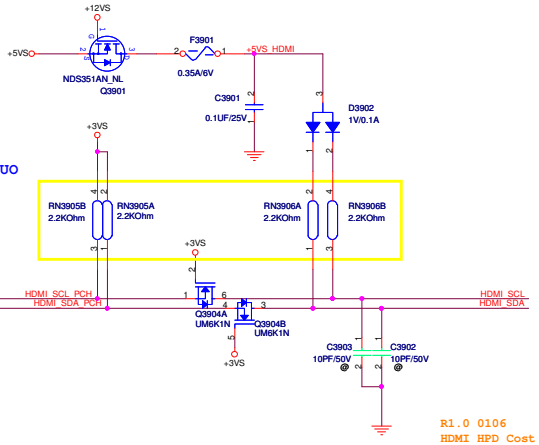




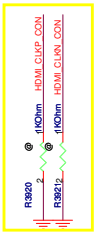


HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible

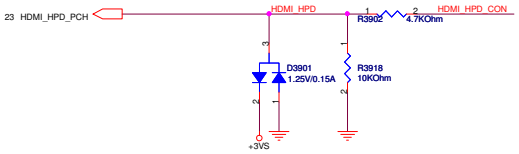




RN3905,RN3906
Intel design guide:2.2K ohm /UMA
NV reference schematics:4.7K ohm /DGPUO



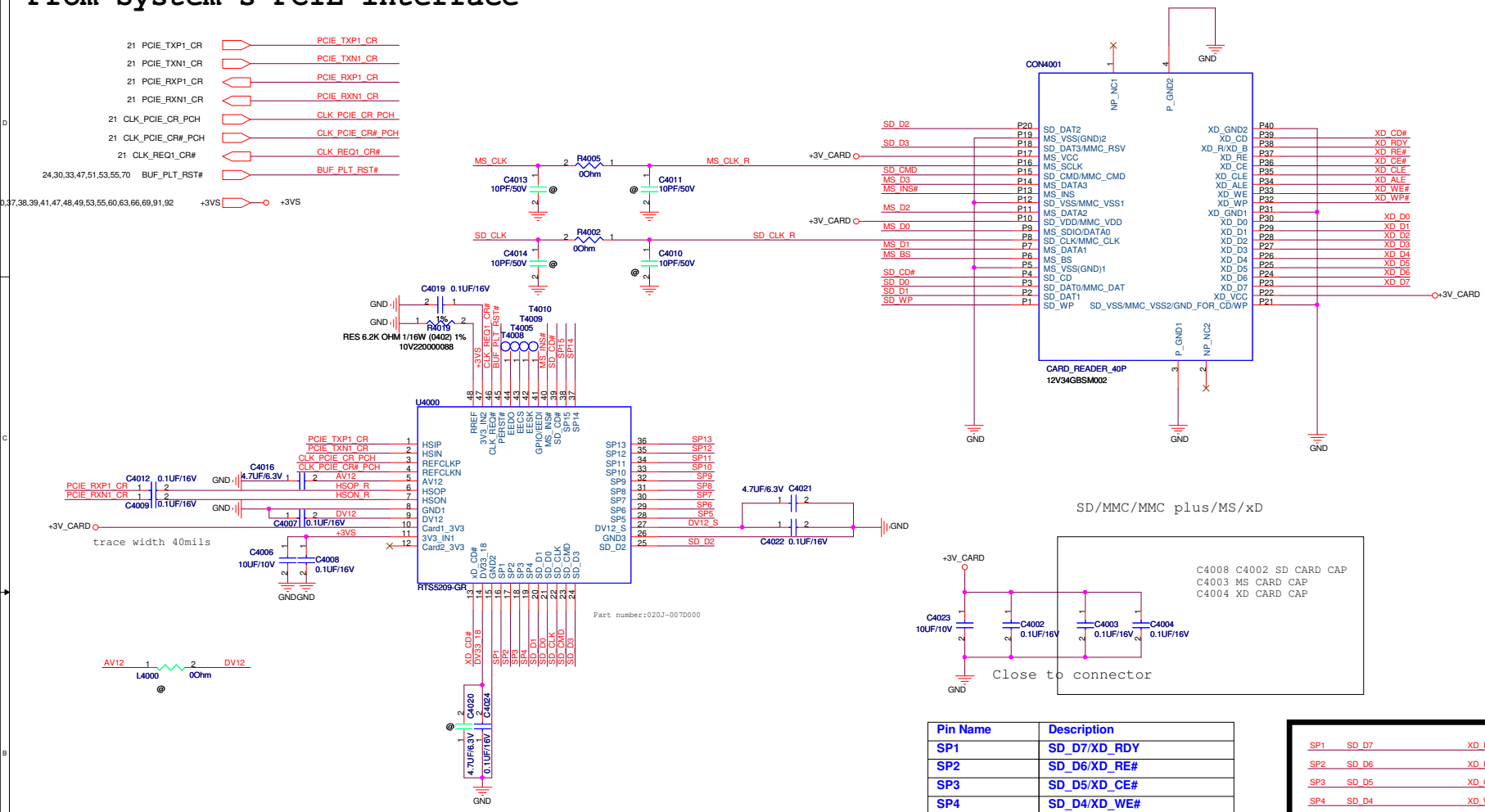
EMI solution



R1.0 0106
HDMI HPD Cost Reduced Level Shifter Design Recommendation

PEGATRON Title : HDMI
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng
Size: Custom | Project Name: BA52HR/CR | Rev: 1.0
Date: Friday, February 03, 2012 Sheet 39 of 77

From System's PCIE interface



Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

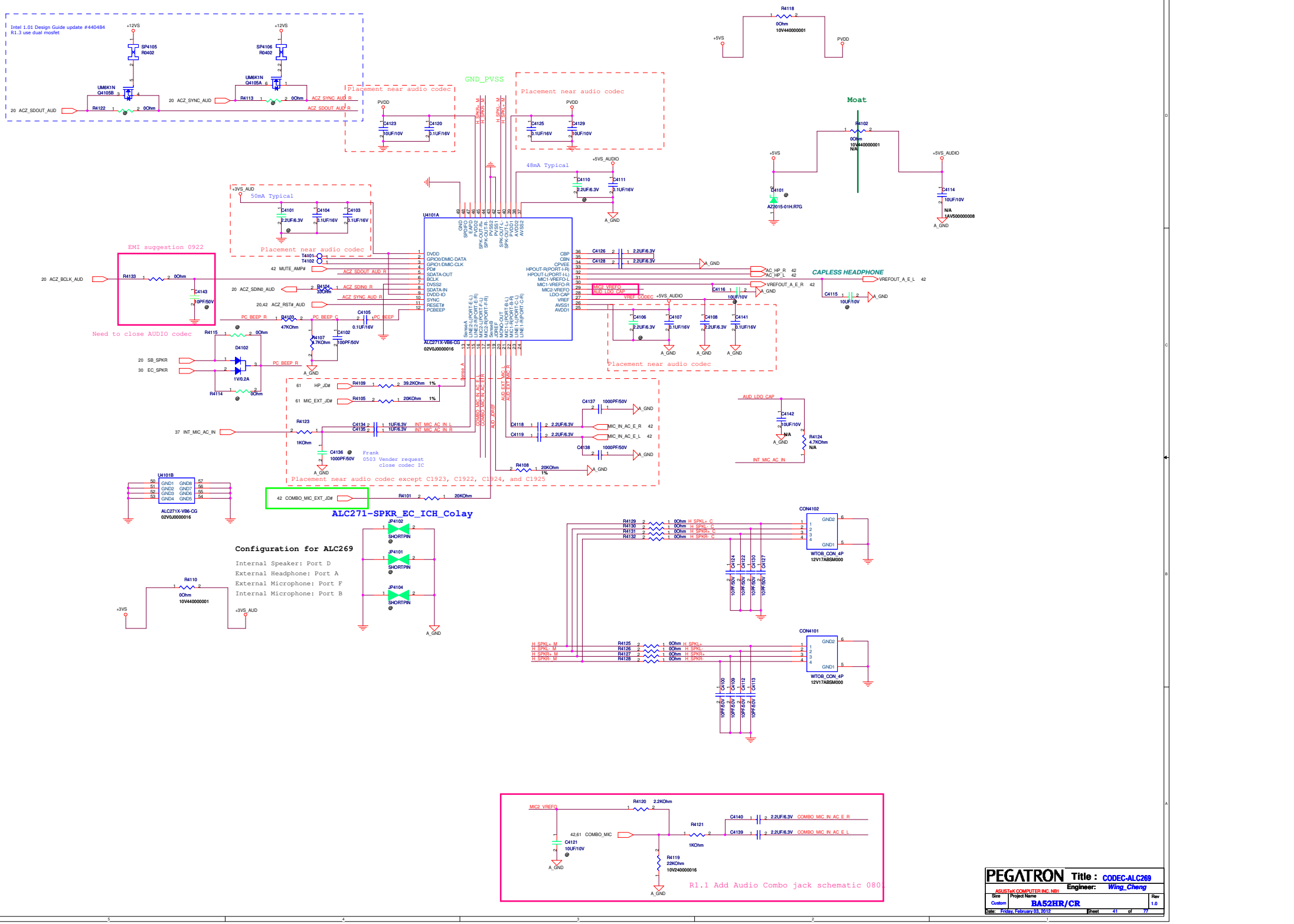
Share Pin

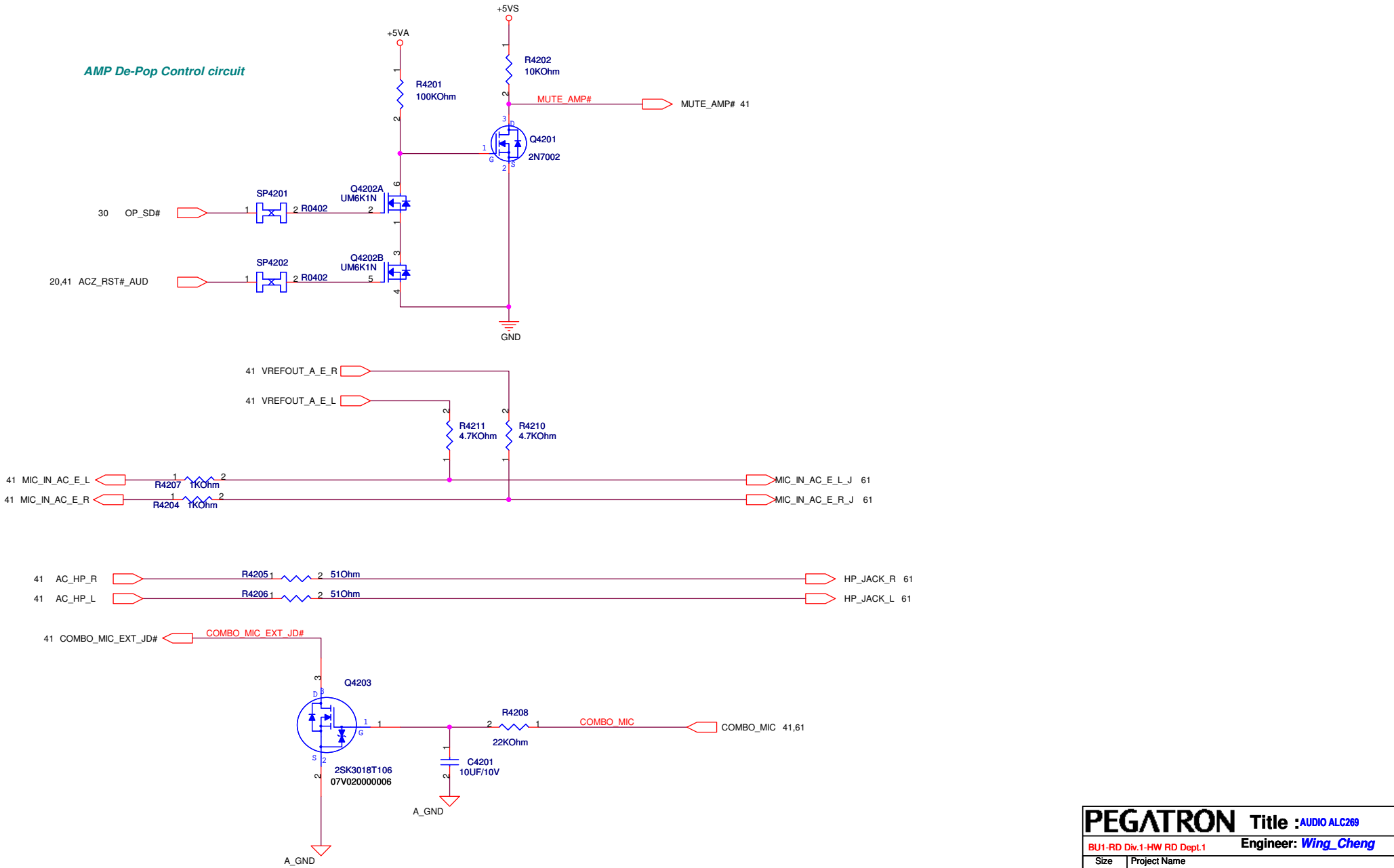
PEGATRON Title : RTS5209

BG1/CSC/HW5 Engineer: Peter5 Huang

Size: Custom | Project Name: Comal | Rev: 1.0

Date: Friday, February 03, 2012 | Sheet 40 of 99


Intel 1.01 Design Guide update #440484
R1.3 use dual mosfet
Placement near audio codec
GND_PVSS
48mA Typical
50mA Typical
Moat
EMI suggestion 0922
Need to close AUDIO codec
CAPLESS HEADPHONE
ALC271X-VB6-CG
02V0J0000016
Configuration for ALC269
Internal Speaker: Port D
External Headphone: Port A
External Microphone: Port F
Internal Microphone: Port B
ALC271-SPKR_EC_ICH_Colay
Frank
0503 Vender request
close codec IC
R1.1 Add Audio Combo jack schematic 080
PEGATRON
Title : CODEC-ALC269
Engineer: Wing_Cheng
ASUSTeK COMPUTER INC. NB1
BA52HR/CR
Rev 1.0
Friday, February 03, 2012
Sheet 41 of 77



PEGATRON Title : AUDIO ALC269

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
B	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 42 of 77

PEGATRON Title : MDC CONN

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 43 of 77

Del Entry audio circuit

SR-8
0121-11

PEGATRON Title : CODEC-ALC269

ASUSTeK COMPUTER INC. NB1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 44 of 77

Del Entry audio circuit

SR-8
0121-11

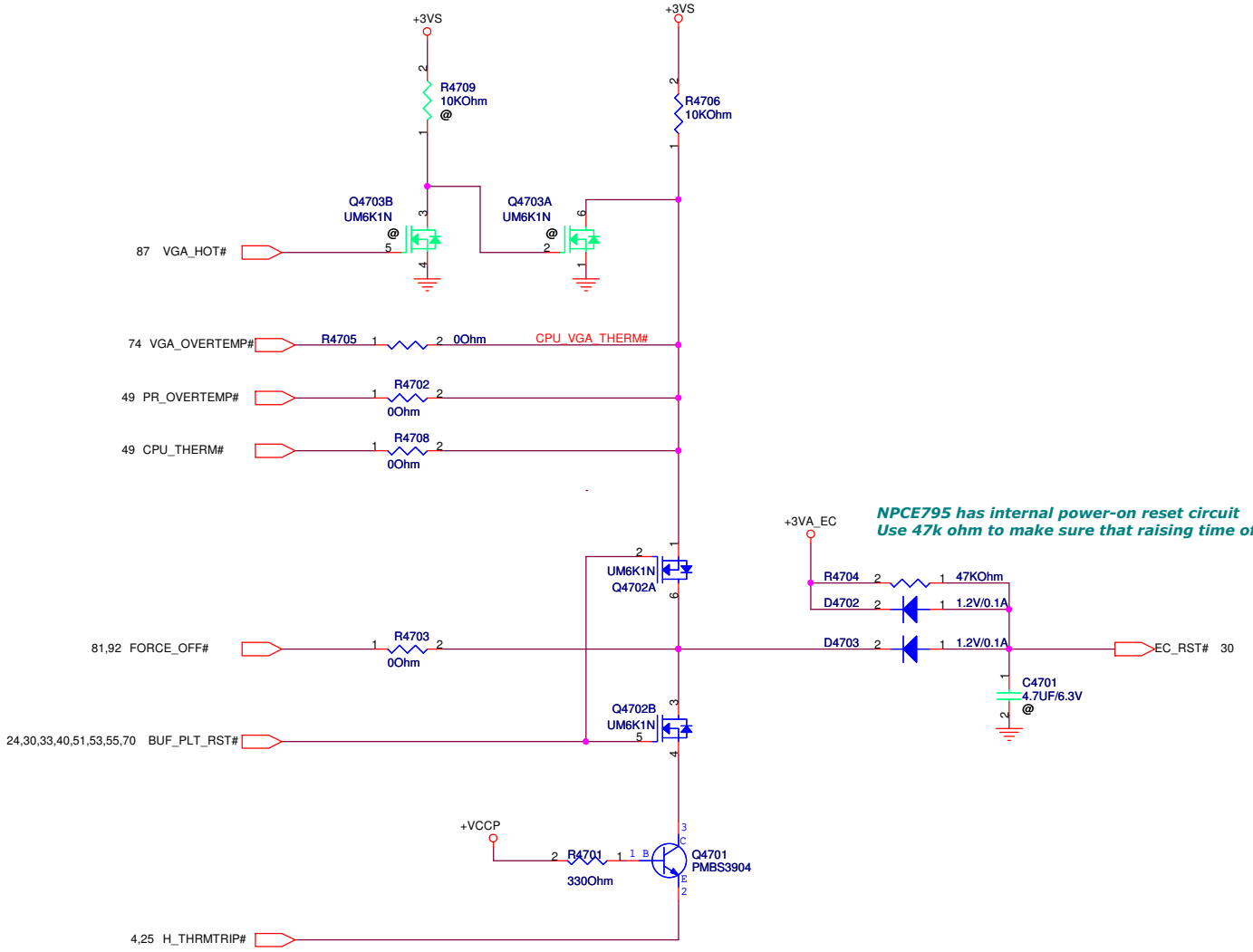
PEGATRON Title : AUDIO ALC269

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 45 of 77

Thermal Policy

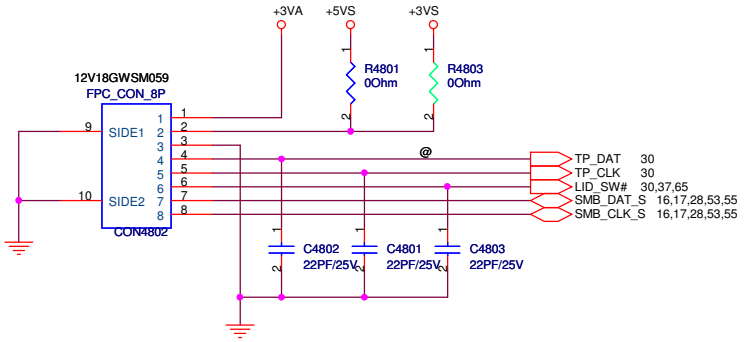


+3VA_EC +3VA_EC 28,30

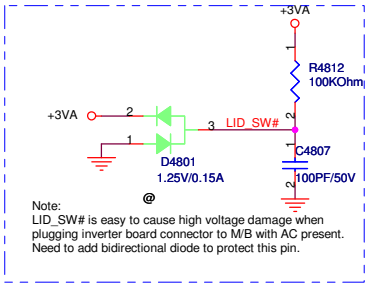
+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,48,49,53,55,60,63,66,69,91,92

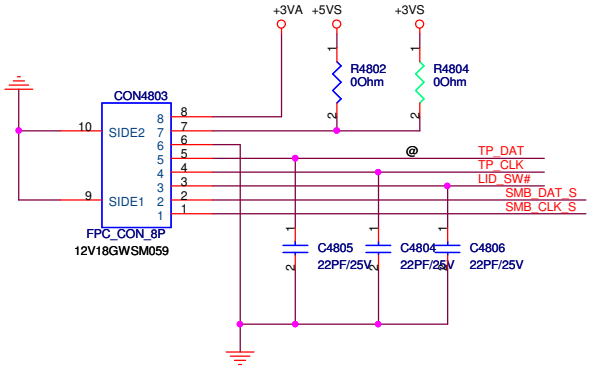
PEGATRON	Title : RST_Reset Circuit	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Wing_Cheng	
Size: B	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, February 03, 2012	Sheet 47 of 77	

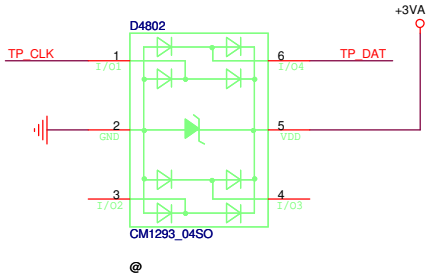
Touch Pad Button/ Hall Sensor



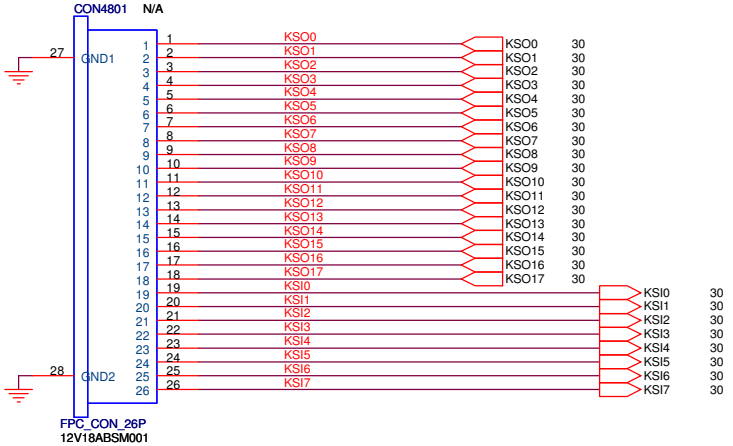
close toU4601



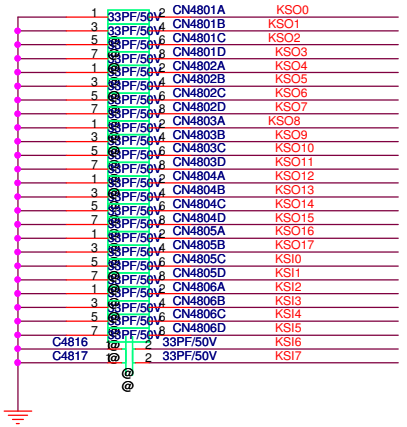




Keyboard



1218-00MW000



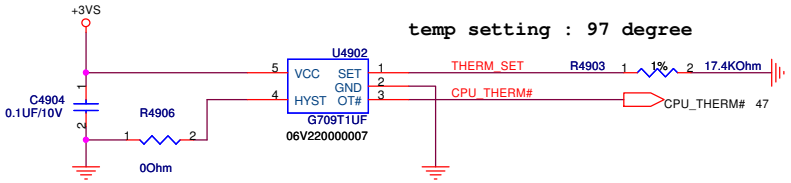
PEGATRON Title : KB/ TP/ FLASH

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

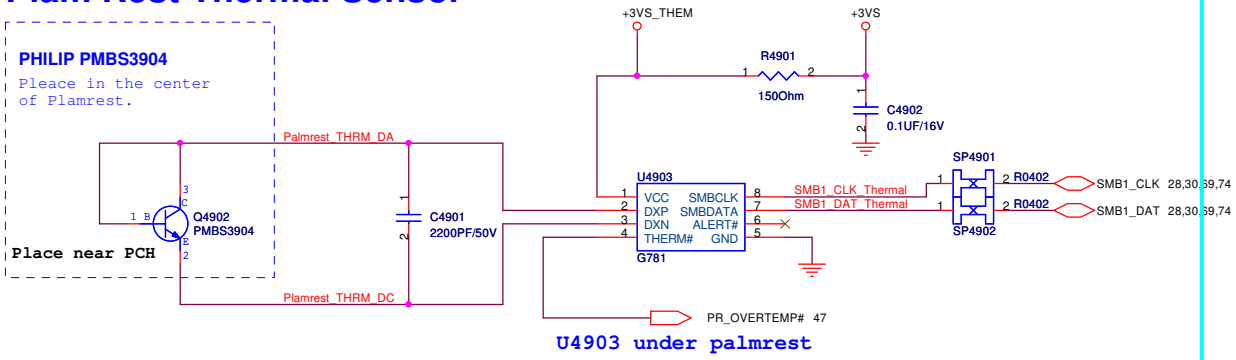
Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 48 of 77

U5001 Close to CPU



Plam Rest Thermal Sensor



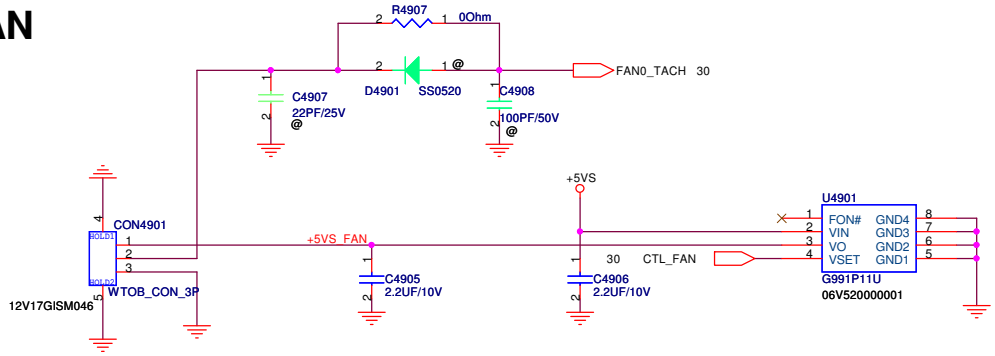
U4903 under palmrest

SMBUS addr=1001100x (98)

U4903: Remote(Local) thermal sensor,use remote mode.

R1.2-10

FAN



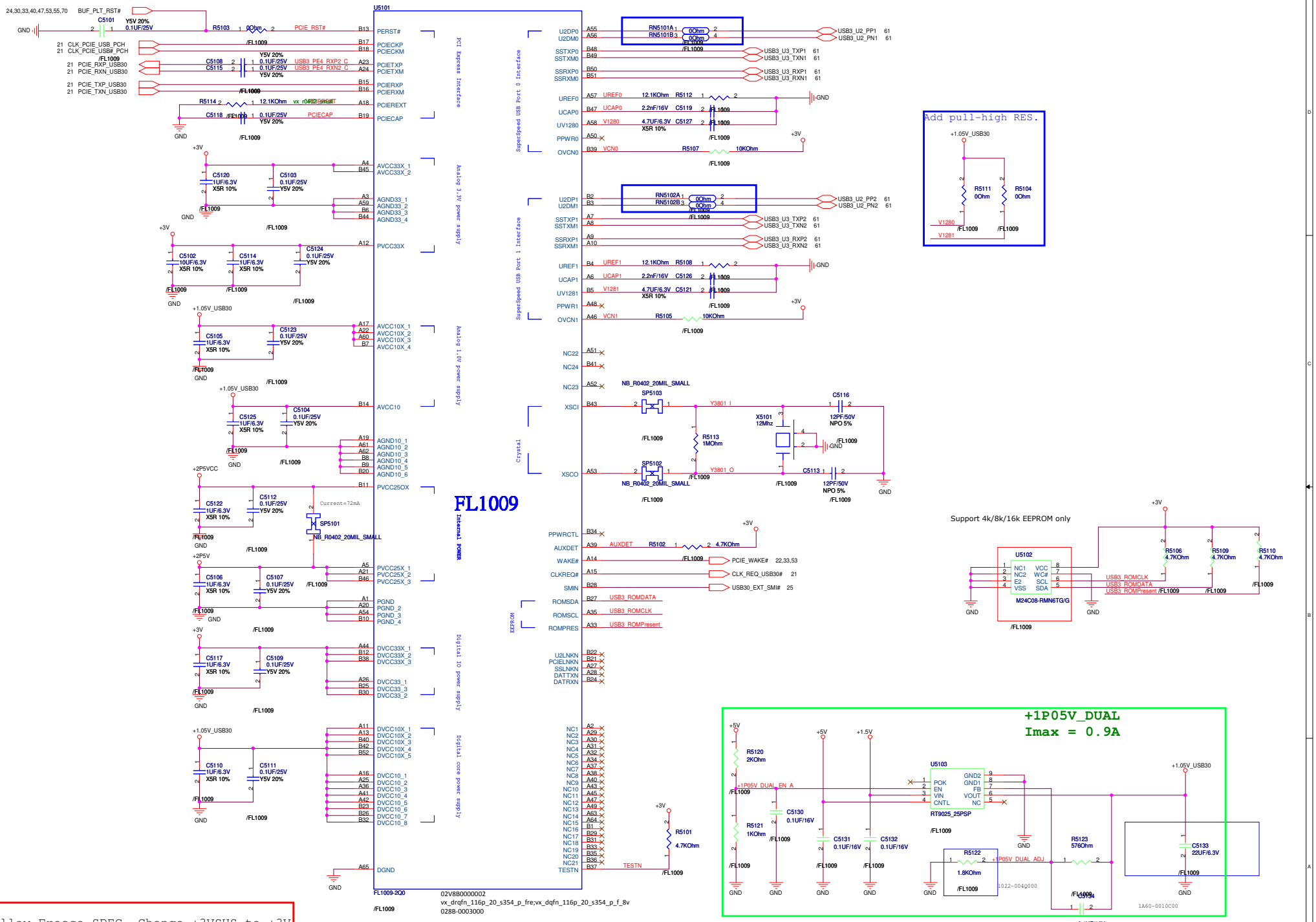
PEGATRON	Title : THERMAL/ FAN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, February 03, 2012	Sheet 49 of 77	

PEGATRON Title : Realtek_RTS5138

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 50 of 77


U5101
FL1009
Internal POWER
PCI Express Interface
SuperSpeed USB Port 0 Interface
SuperSpeed USB Port 1 Interface
Analog 3.3V power supply
Analog 1.0V power supply
Crystal
EEPROM
Digital IO power supply
Digital core power supply
PERST#
PCIECKP
PCIECKM
PCIETXP
PCIETXM
PCIERXP
PCIERXM
PCIEREXT
PCIECAP
AVCC33X_1
AVCC33X_2
AGND33_1
AGND33_2
AGND33_3
AGND33_4
PVCC33X
AVCC10X_1
AVCC10X_2
AVCC10X_3
AVCC10X_4
AVCC10
AGND10_1
AGND10_2
AGND10_3
AGND10_4
AGND10_5
AGND10_6
PVCC25OX
PVCC25X_1
PVCC25X_2
PVCC25X_3
PGND
PGND_2
PGND_3
PGND_4
DVCC33X_1
DVCC33X_2
DVCC33X_3
DVCC33_1
DVCC33_3
DVCC33_2
DVCC10X_1
DVCC10X_2
DVCC10X_3
DVCC10X_4
DVCC10X_5
DVCC10_1
DVCC10_2
DVCC10_3
DVCC10_4
DVCC10_5
DVCC10_6
DVCC10_7
DVCC10_8
DGND
U2DP0
U2DM0
SSTXP0
SSTXM0
SSRXP0
SSRXM0
UREF0
UCAP0
UV1280
PPWR0
OVCN0
U2DP1
U2DM1
SSTXP1
SSTXM1
SSRXP1
SSRXM1
UREF1
UCAP1
UV1281
PPWR1
OVCN1
NC22
NC24
NC23
XSCI
XSCO
PPWRCTL
AUXDET
WAKE#
CLKREQ#
SMIN
ROMSDA
ROMSCL
ROMPRES
U2LNKN
PCIELNKN
SSLNKN
DATTXN
DATRXN
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18
NC19
NC20
NC21
TESTN
FL1009-2Q0
02V8B0000002
vx_drqfn_116p_20_s354_p_fre;vx_dqfn_116p_20_s354_p_f_8v
028B-0003000
Add pull-high RES.
Support 4k/8k/16k EEPROM only
M24C08-RMN6TG/G
+1P05V_DUAL
Imax = 0.9A
RT9025_25PSP
Follow Fresco SPEC, Change +3VSUS to +3V
(1.05v must not be removed earlier then
3.3V supply removed.)
PEGATRON
Title : USB3.0 uPD720200
Engineer: Wing_Cheng
BG1\HW1
Size C
Project Name BA52HR/CR
Rev 1.0
Date: Friday, February 03, 2012
Sheet 51 of 77

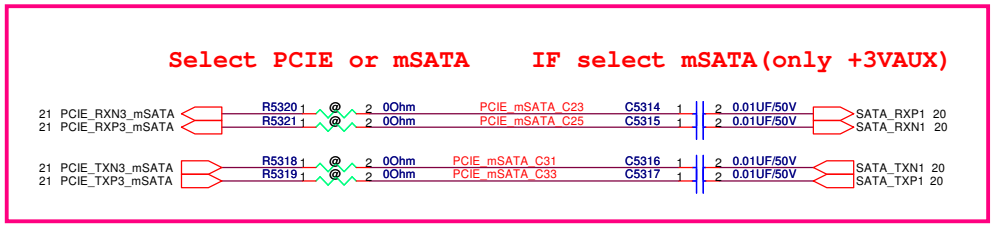
PEGATRON Title : PCIE NEW CARD

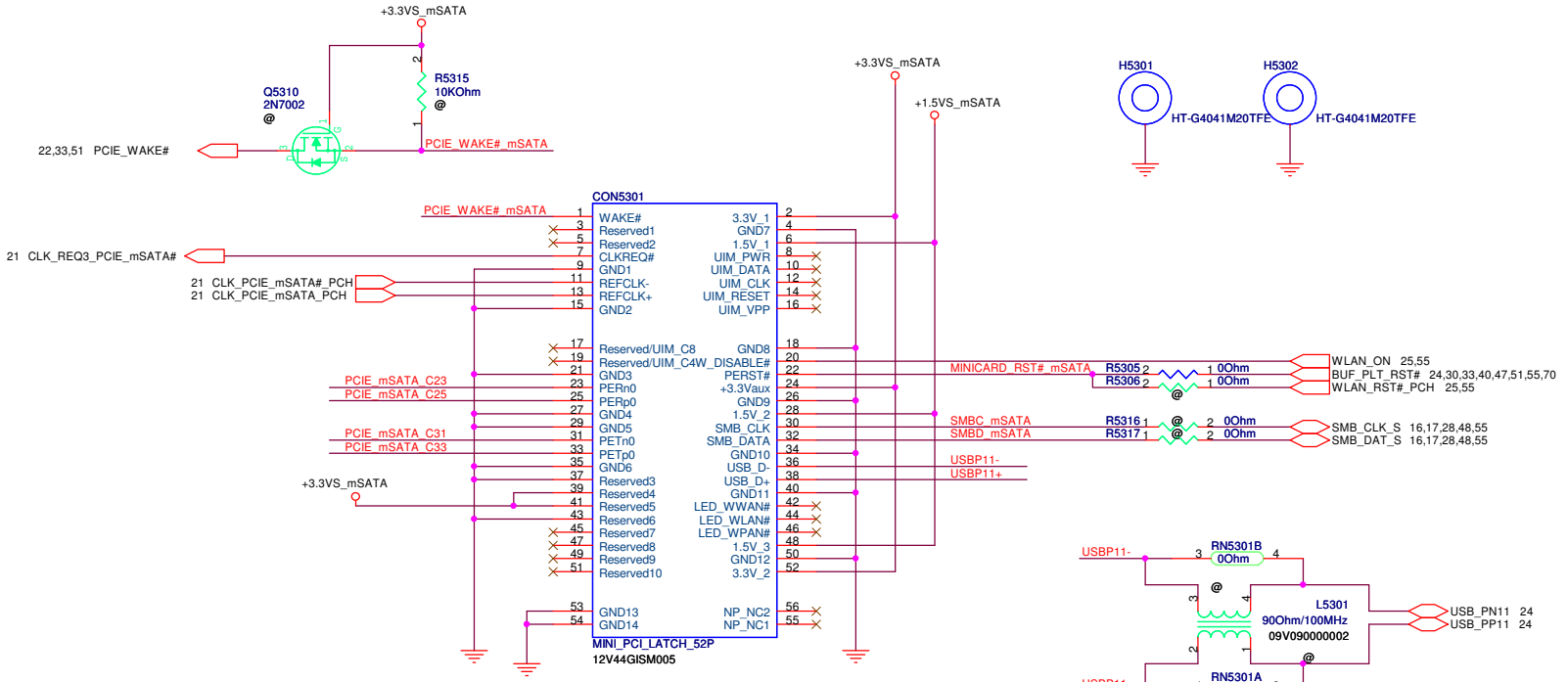
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

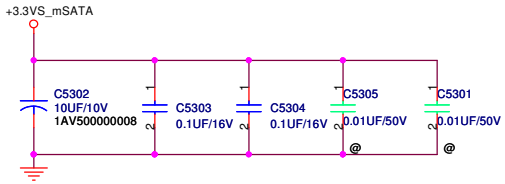
Size	Project Name	Rev
Custom	BA52HR/CR	1.0

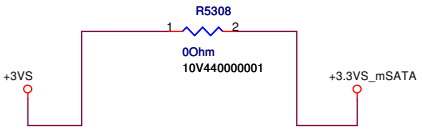
Date: Friday, February 03, 2012 Sheet 52 of 77

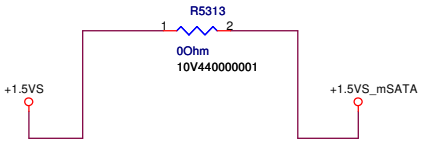
PCIE/mSATA

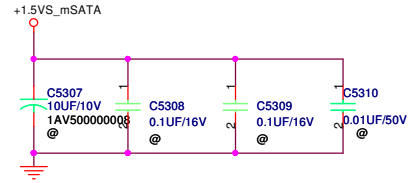












PEGATRON	Title : WiFi/WiMAX	
BU1-RD Div.1-HW RD Dept.1	Engineer:	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, February 03, 2012	Sheet 53 of 77	

PEGATRON

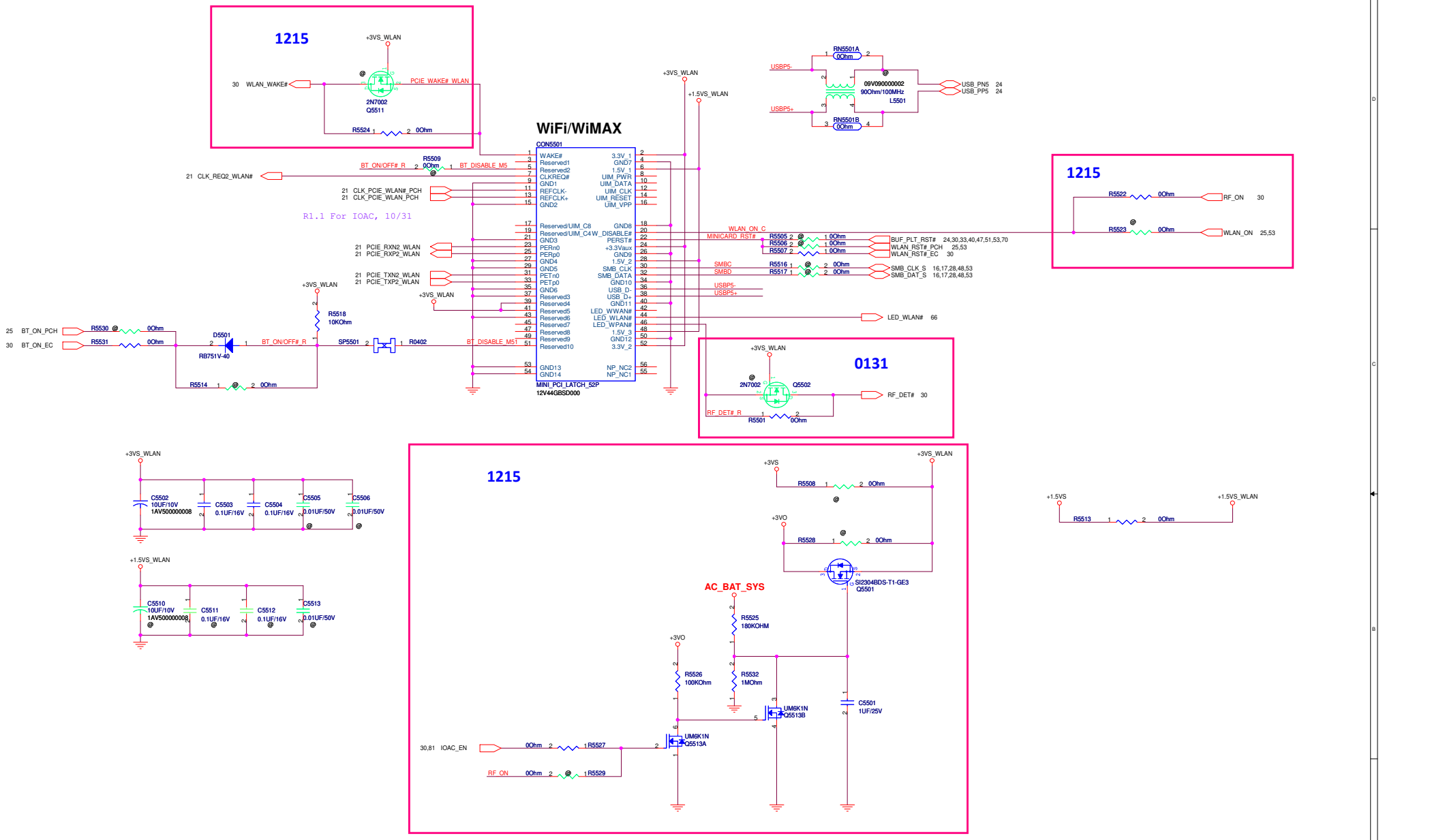
Title : MINICARD (WUSB /UPCONVERT)

BU1-RD Div.1-HW RD Dept.1

Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 54 of 77

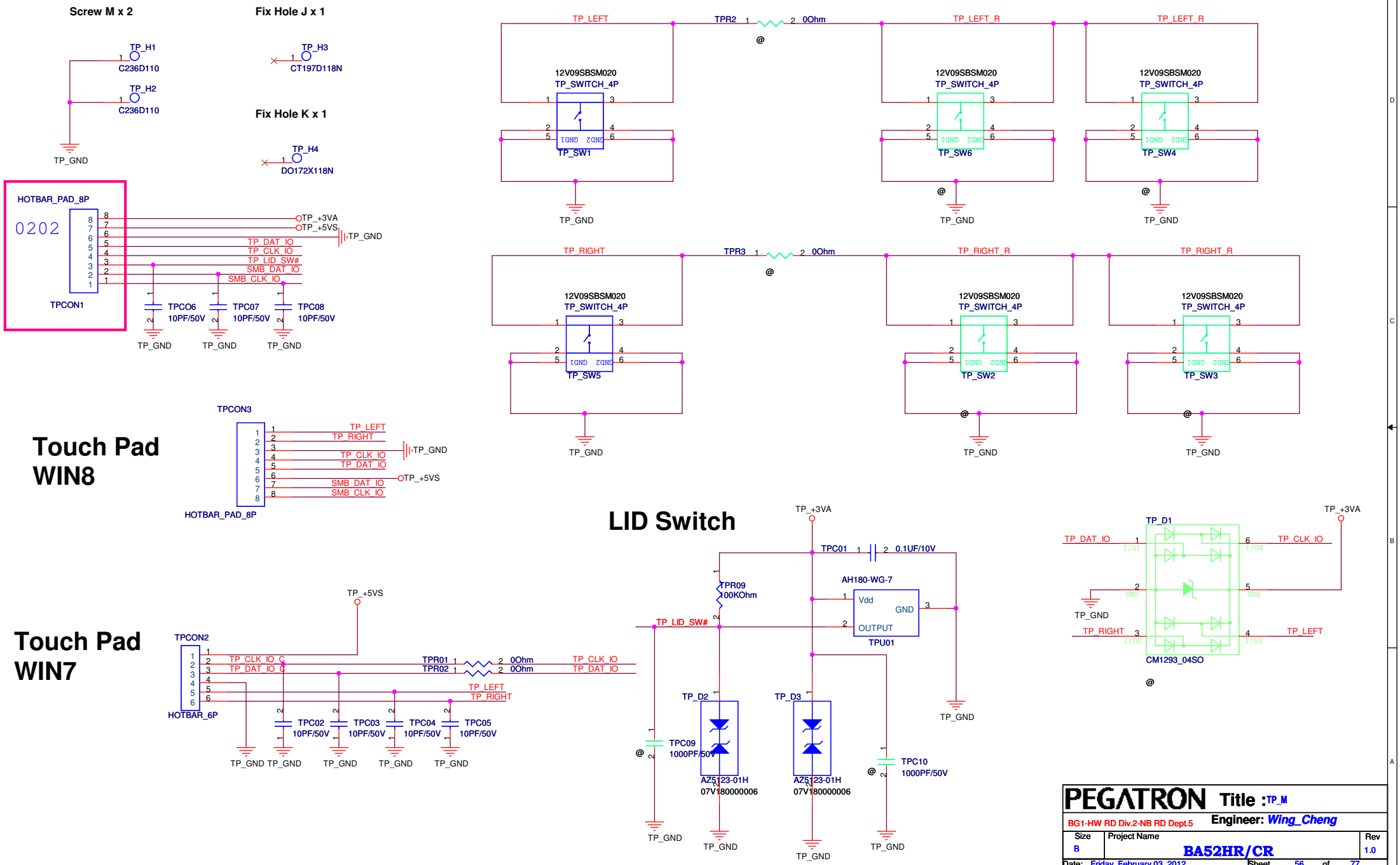


PEGATRON Title : WIFIWIMAX

BU1-RD Div.1-HW RD Dept.1 Engineer:

Size	Project Name	Rev
C	VA70	1.0

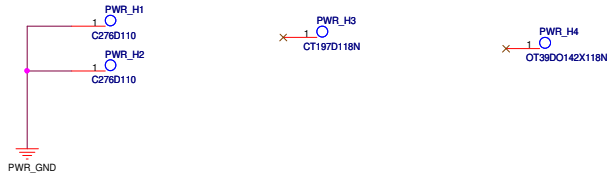
Date: Friday, February 03, 2012 Sheet 55 of 77


Screw M x 2
TP_H1
C236D110
TP_H2
C236D110
TP_GND
Fix Hole J x 1
TP_H3
CT197D118N
Fix Hole K x 1
TP_H4
DO172X118N
HOTBAR_PAD_8P
0202
TPCON1
TP_+3VA
TP_+5VS
TP_GND
TP_DAT_IO
TP_CLK_IO
TP_LID_SW#
SMB_DAT_IO
SMB_CLK_IO
TPC06 10PF/50V
TPC07 10PF/50V
TPC08 10PF/50V
TP_LEFT
TPR2 0Ohm
TP_LEFT_R
12V09SBSM020
TP_SWITCH_4P
TP_SW1
TP_SW6
TP_SW4
TP_RIGHT
TPR3 0Ohm
TP_RIGHT_R
TP_SW5
TP_SW2
TP_SW3
Touch Pad WIN8
TPCON3
HOTBAR_PAD_8P
Touch Pad WIN7
TPCON2
HOTBAR_6P
TPR01 0Ohm
TPR02 0Ohm
TP_CLK_IO_C
TP_DAT_IO_C
TPC02 10PF/50V
TPC03 10PF/50V
TPC04 10PF/50V
TPC05 10PF/50V
LID Switch
TPC01 0.1UF/10V
TPR09 100KOhm
AH180-WG-7
Vdd
GND
OUTPUT
TPU01
TP_D2
TP_D3
AZ5123-01H
07V180000006
TPC09 1000PF/50V
TPC10 1000PF/50V
TP_D1
CM1293_04SO
PEGATRON
Title :TP_M
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Wing_Cheng
Size B
Project Name BA52HR/CR
Rev 1.0
Date: Friday, February 03, 2012
Sheet 56 of 77

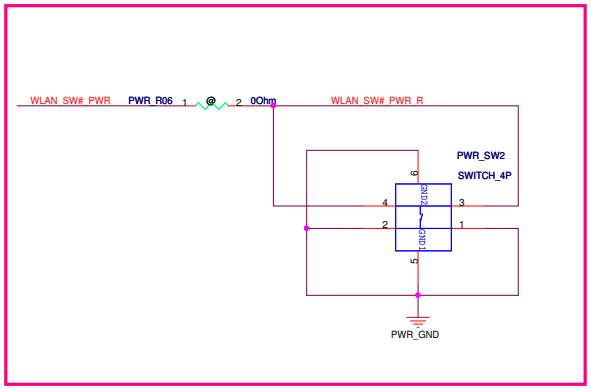
Screw G x 2

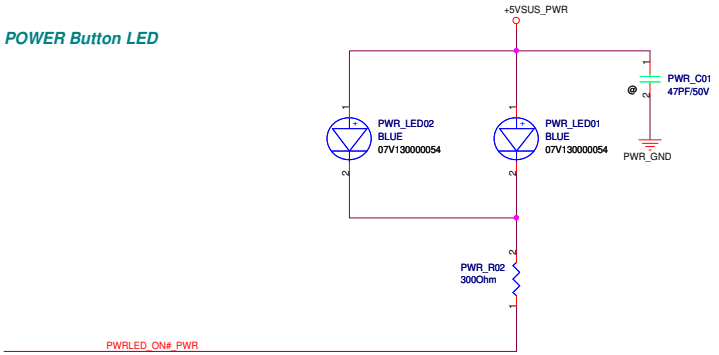
Fix Hole H x 1

Fix Hole I x 1

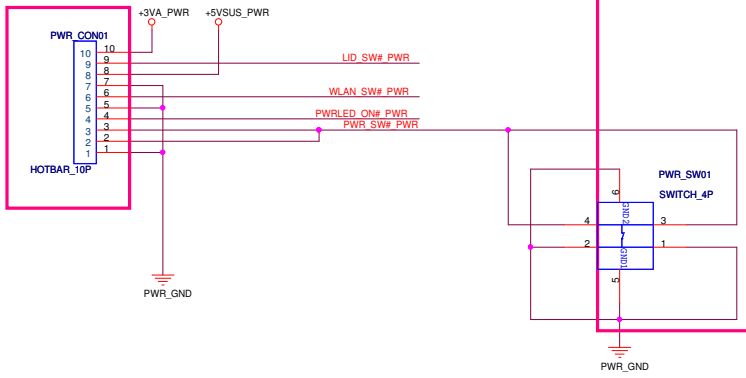


POWER Button LED

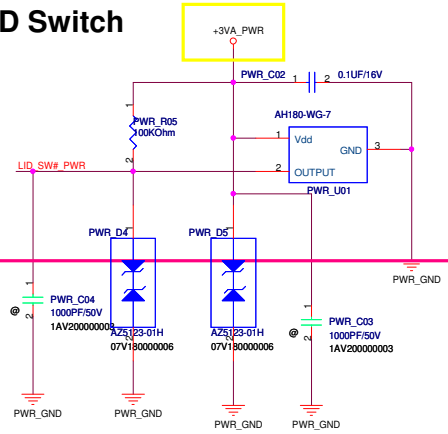


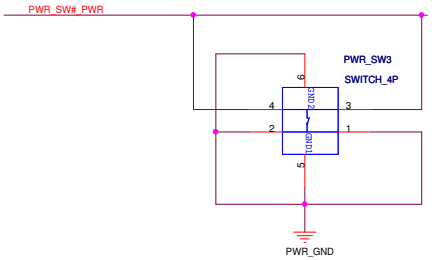


R1.1 reverse PWR_CON01 and change pin 1~4 pin define 1024

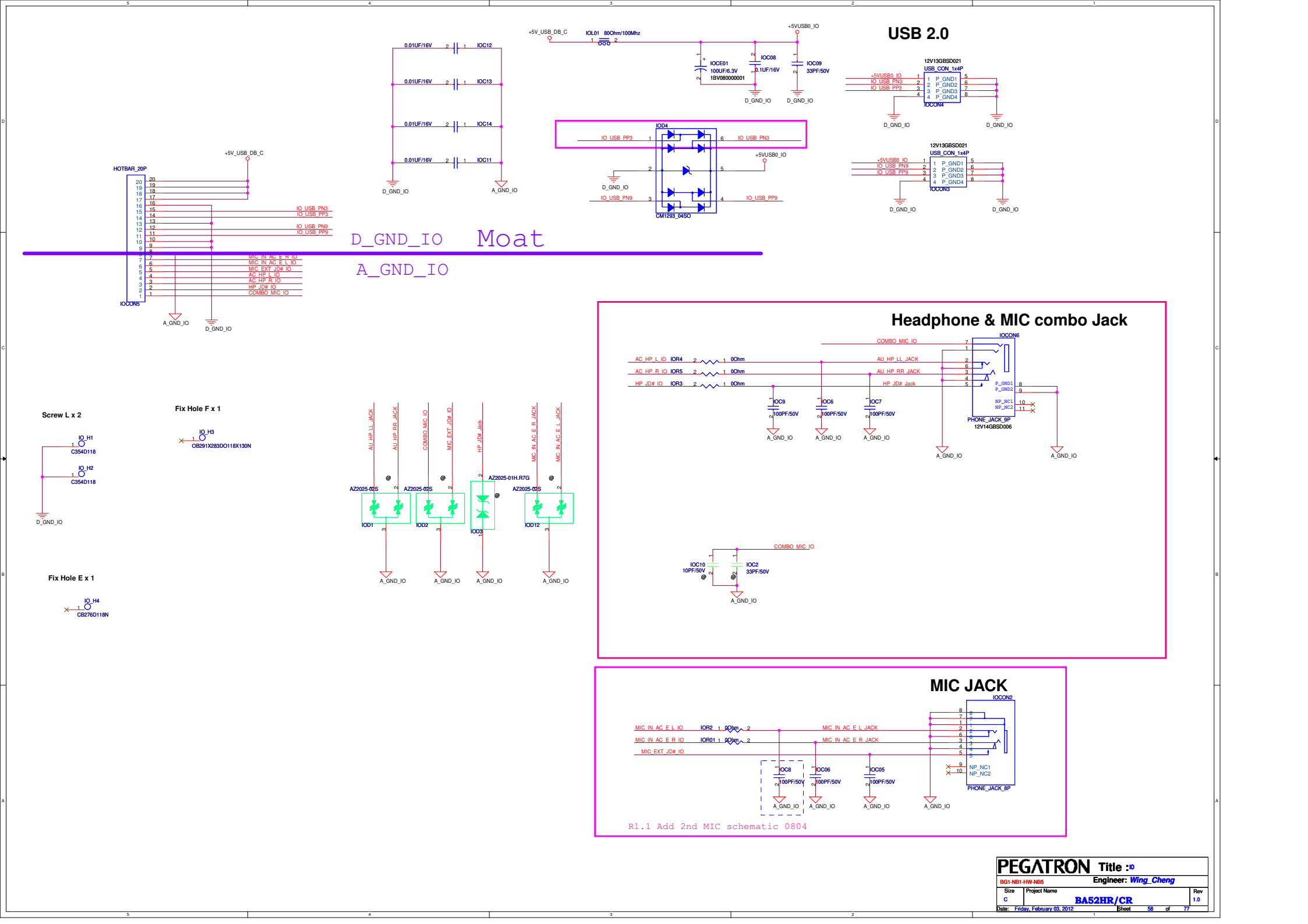


LID Switch





PEGATRON	Title : PWR BTN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, February 03, 2012	Sheet 57 of 77	


USB 2.0
+5V_USB_DB_C
IOL01 80Ohm/100Mhz
+5VUSB0_IO
IOCE01
100UF/6.3V
1BV080000001
IOC08
0.1UF/16V
IOC09
33PF/50V
D_GND_IO
12V13GBSD021
USB_CON_1x4P
IO_USB_PN3
IO_USB_PP3
IO_USB_PN9
IO_USB_PP9
IOCON4
IOCON3
IOD4
CM1293_04SO
HOTBAR_20P
IOCON5
0.01UF/16V
IOC12
IOC13
IOC14
IOC11
A_GND_IO
D_GND_IO
Moat
MIC_IN_AC_E_R_IO
MIC_IN_AC_E_L_IO
MIC_EXT_JD#_IO
AC_HP_L_IO
AC_HP_R_IO
HP_JD#_IO
COMBO_MIC_IO
Screw L x 2
Fix Hole F x 1
Fix Hole E x 1
IO_H1
IO_H2
IO_H3
IO_H4
C354D118
OB291X283DO118X130N
CB276D118N
Headphone & MIC combo Jack
IOCON6
AC_HP_L_IO IOR4
AC_HP_R_IO IOR5
HP_JD#_IO IOR3
0Ohm
AU_HP_LL_JACK
AU_HP_RR_JACK
HP_JD#_Jack
IOC9
IOC6
IOC7
100PF/50V
PHONE_JACK_9P
12V14GBSD006
P_GND1
P_GND2
NP_NC1
NP_NC2
AZ2025-02S
AZ2025-01H.R7G
IOD1
IOD2
IOD3
IOD12
IOC10
10PF/50V
IOC2
33PF/50V
MIC JACK
IOCON2
MIC_IN_AC_E_L_IO
MIC_IN_AC_E_R_IO
MIC_EXT_JD#_IO
IOR2
IOR01
MIC_IN_AC_E_L_JACK
MIC_IN_AC_E_R_JACK
IOC8
IOC06
IOC05
PHONE_JACK_8P
R1.1 Add 2nd MIC schematic 0804
PEGATRON
Title :IO
BG1-NB1-HW-NB5
Engineer: Wing_Cheng
Size C
Project Name BA52HR/CR
Rev 1.0
Date: Friday, February 03, 2012
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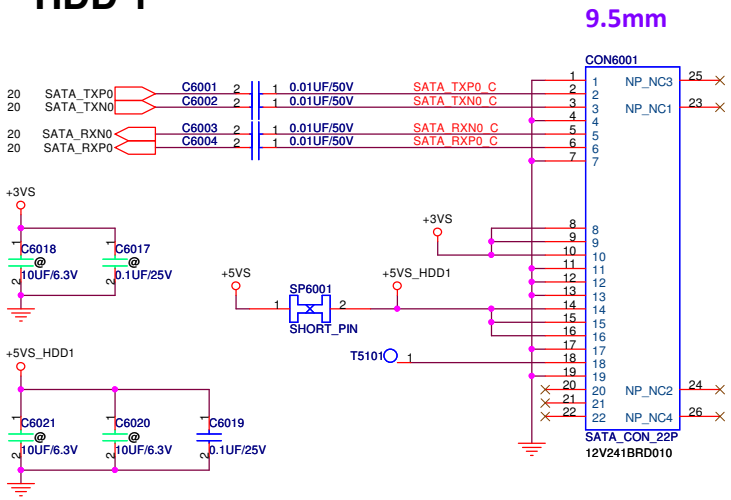
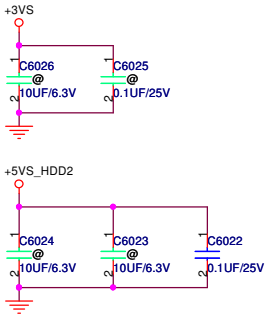
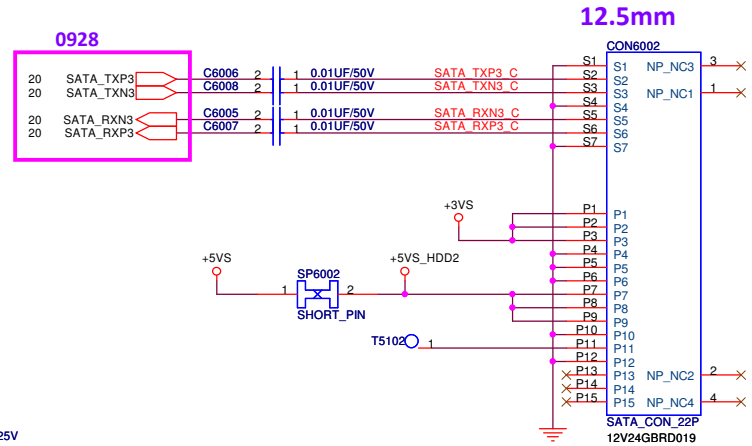
PEGATRON	Title : SLIDE_SW
BU1-RD Div.1-HW RD Dept.1	Engineer: *Wing_Cheng*
Size: A	Project Name: **BA52HR/CR**
Rev: 1.0	
Date: Friday, February 03, 2012	Sheet 59 of 77

HDD 1

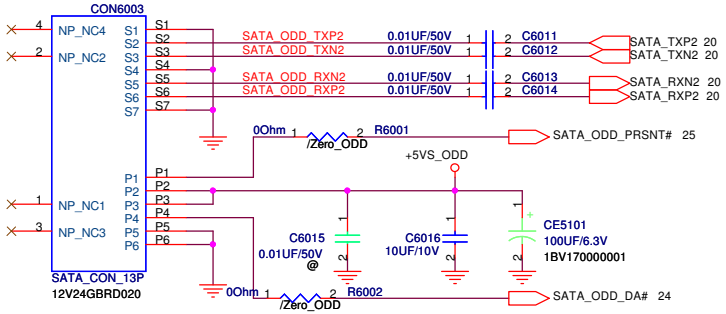




HDD 2

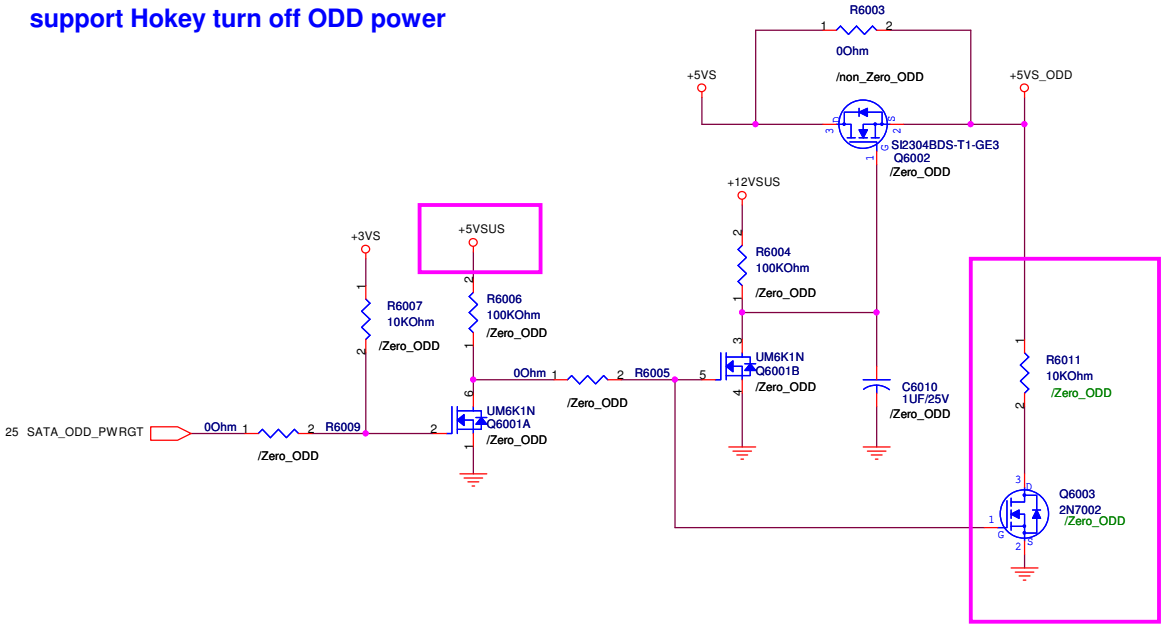


ODD



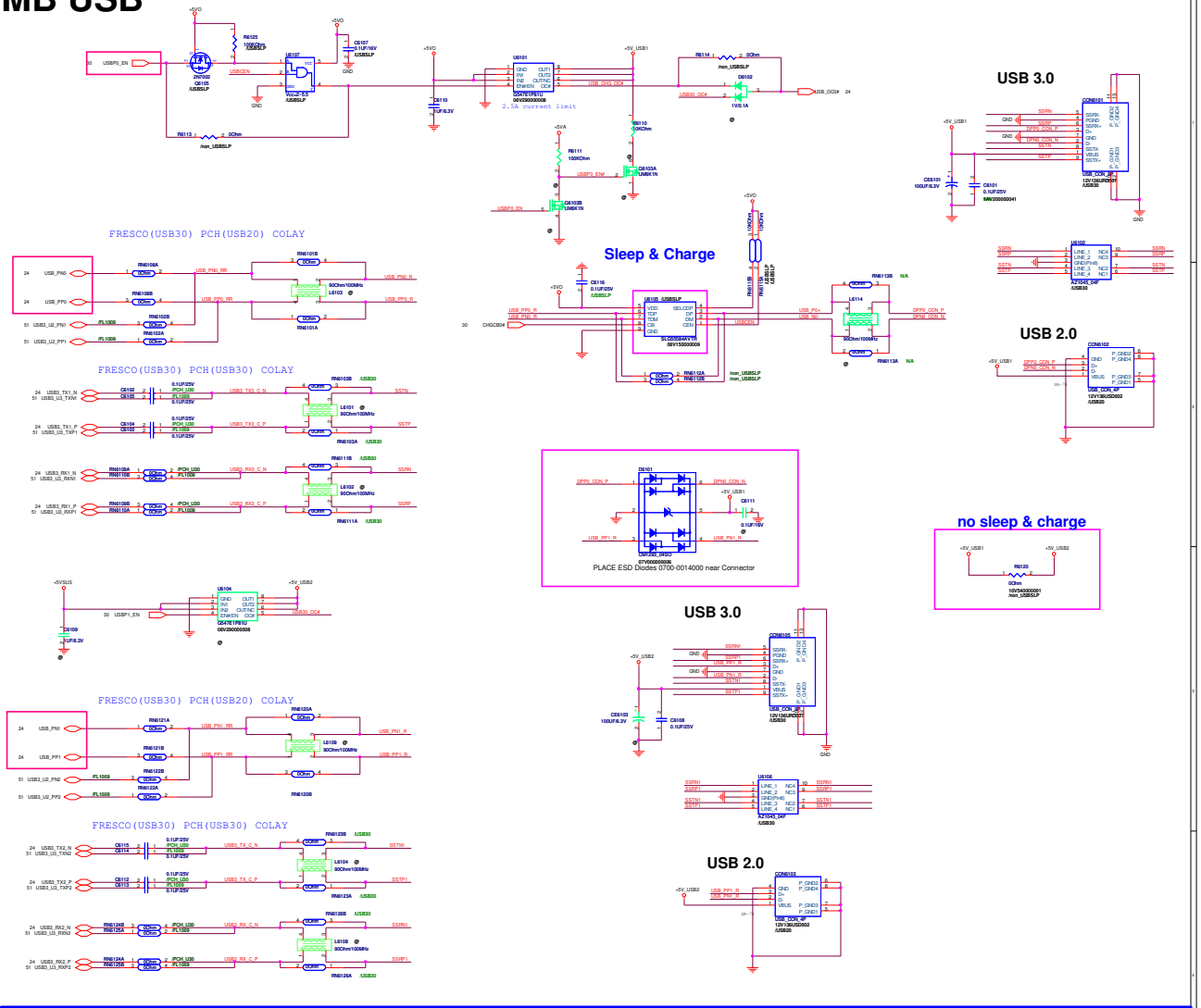
ZERO POWER ODD SUPPORT

support Hokey turn off ODD power

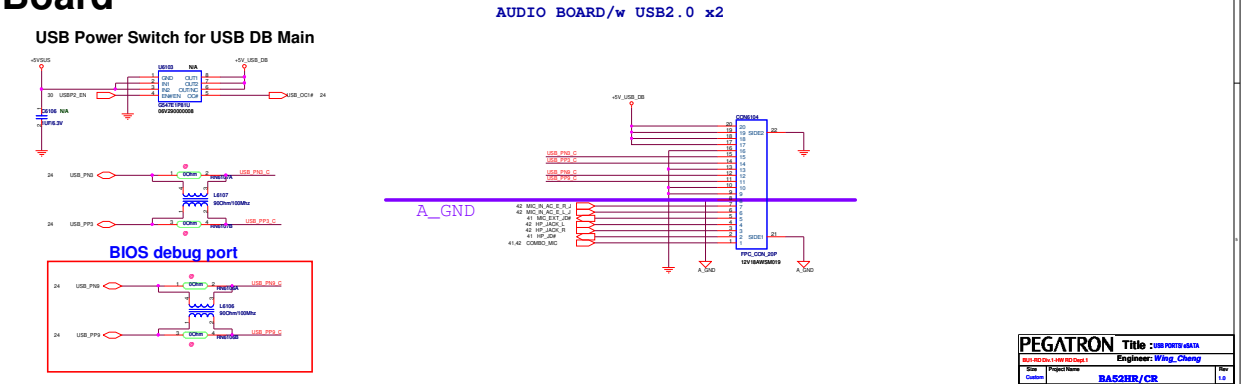


PEGATRON	Title : SATA HDD/ ODD	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, February 03, 2012	Sheet 60 of 77	

MB USB



IO Board



PEGATRON Title : USB PORTR eSATA

Engineer: Wing_Cheng

BA52HR/CR

PEGATRON Title : Camera/ BT/ FL CONN

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

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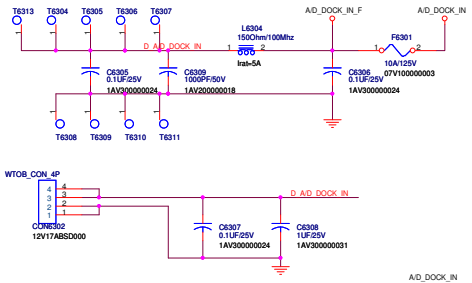
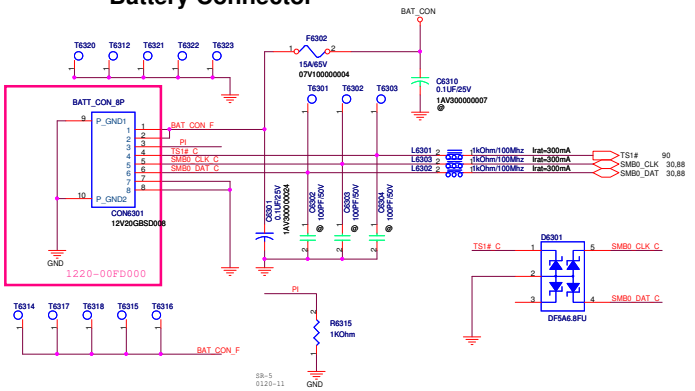
DC IN

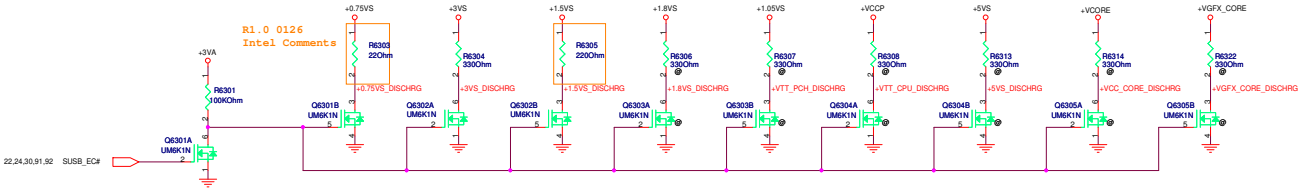


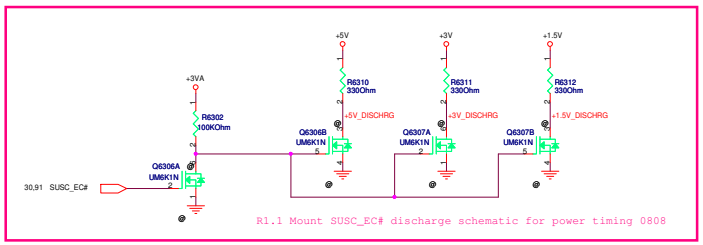
Battery Connector

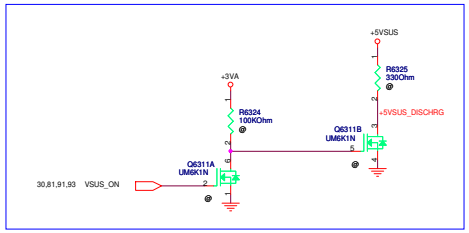


Discharge Circuit

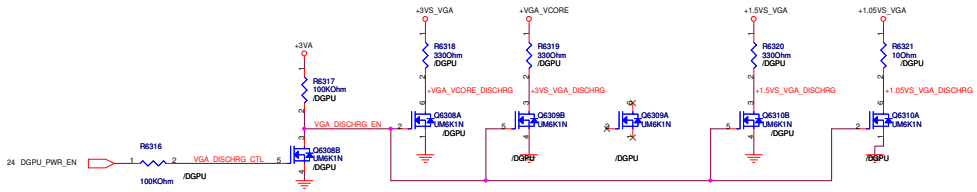
Frank
0505 Follow EVEREST







VGA Discharge Circuit



Unmount +VGA_Vcore discharg

PEGATRON Title : DC-IN/ DISCHARGE
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng
Size: Custom | Project Name: BA52HR/CR | Rev: 1.0
Date: Friday, February 03, 2012 | Sheet 63 of 77

PEGATRON

Title : USB PORTS/ eSATA

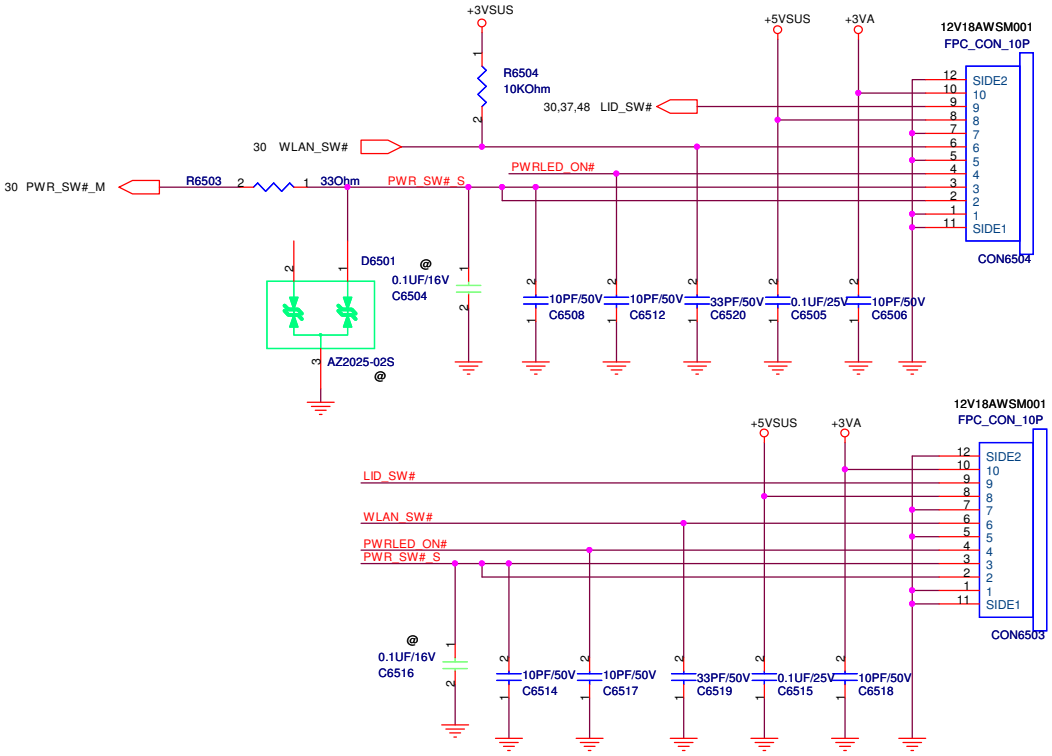
BU1-RD Div.1-HW RD Dept.1

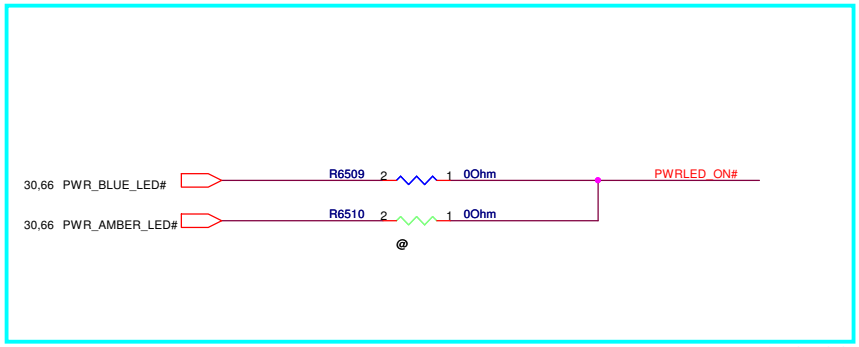
Engineer: *Wing_Cheng*

Size	Project Name	Rev
A	**BA52HR/CR**	1.0

Date: Friday, February 03, 2012 Sheet 64 of 77

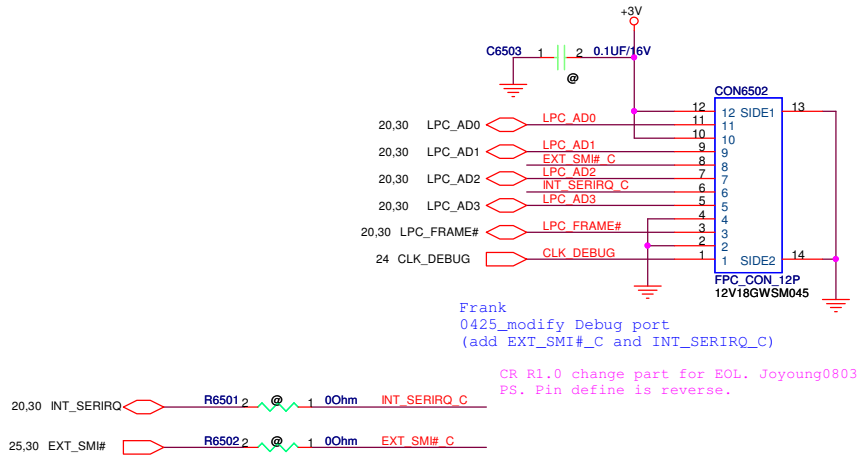
PWR BRD/ AMBIENT/ HALL CONN.





change Power LED CON6503 circuit

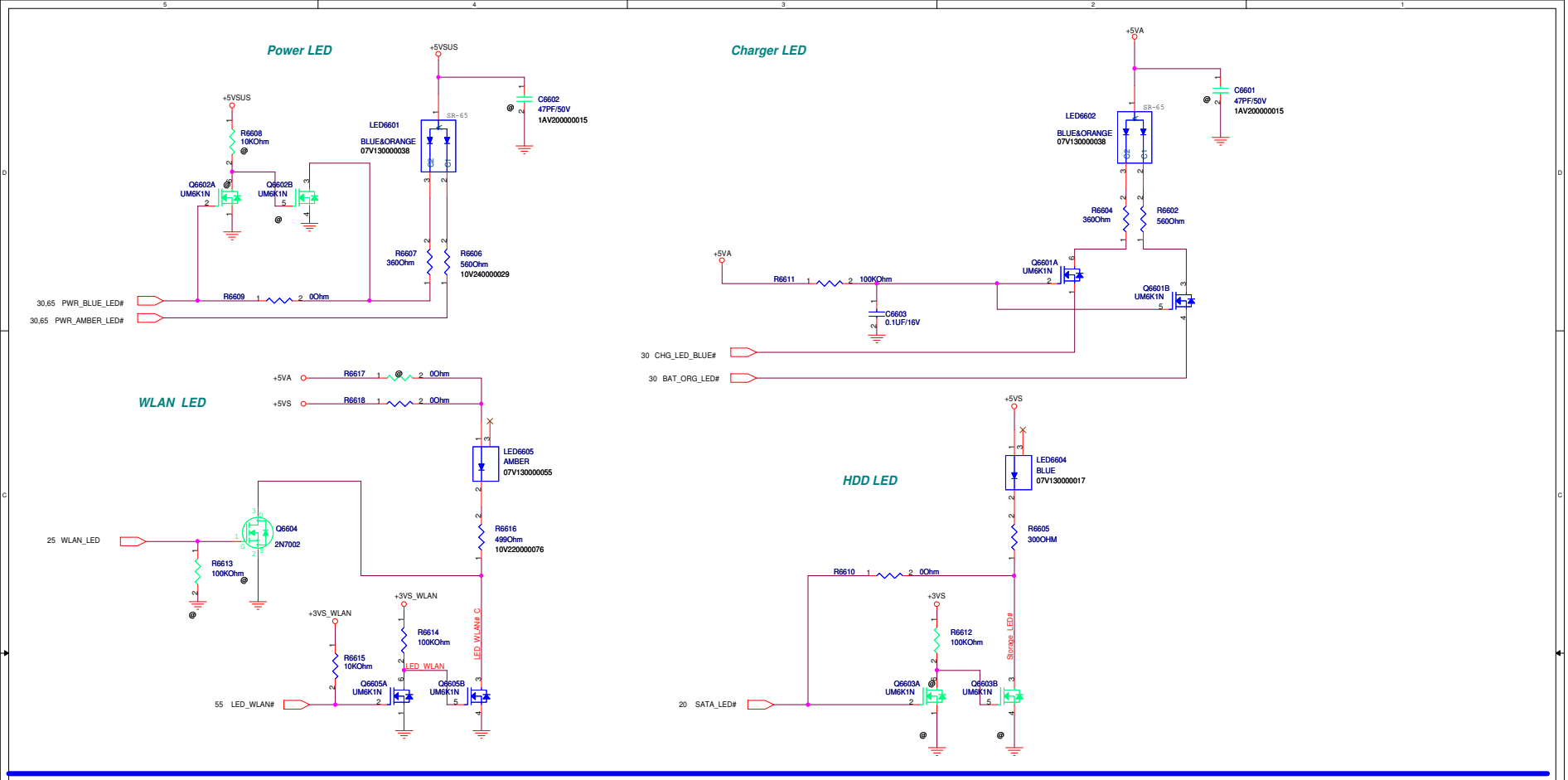
DEBUG CARD CONN.

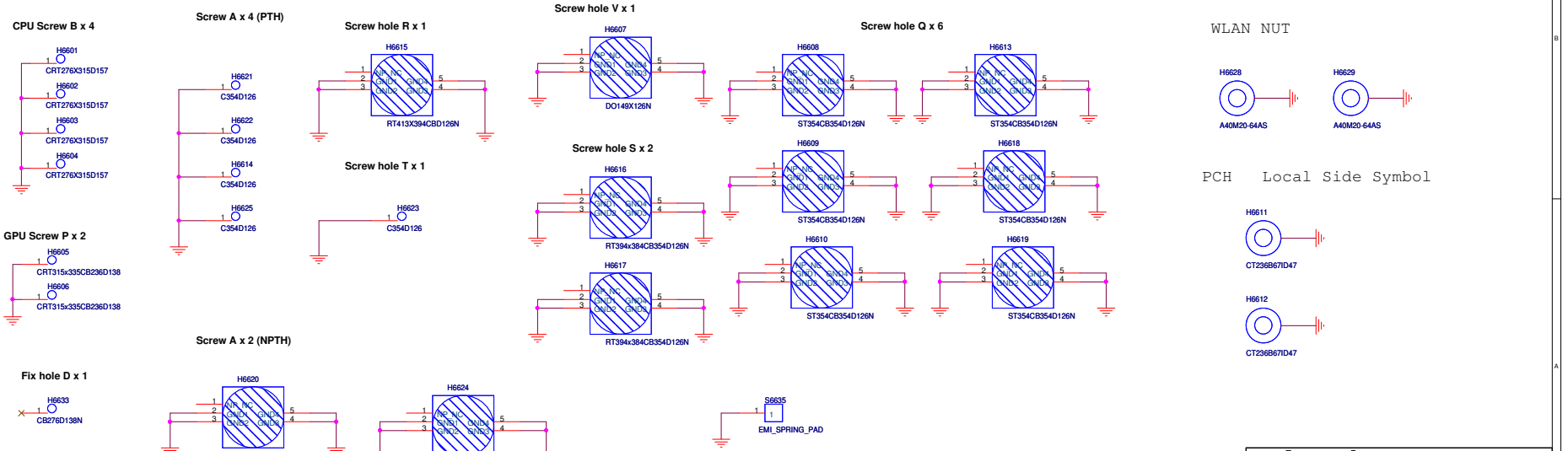


Frank
0425_modify Debug port
(add EXT_SMI#_C and INT_SERIRQ_C)

CR R1.0 change part for EOL. Joyoung0803
PS. Pin define is reverse.

PEGATRON Title : MDC/ PWR SW/ Debug
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng
Size: Custom | Project Name: BA52HR/CR | Rev: 1.0
Date: Friday, February 03, 2012 | Sheet 65 of 77





PEGATRON Title : LED/ CIR/ FN/ SCREW

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

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PEGATRON Title : TPM

Pegatron Corp. Engineer: Wing_Cheng

Size	Project Name	Rev
B	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 67 of 77

PEGATRON

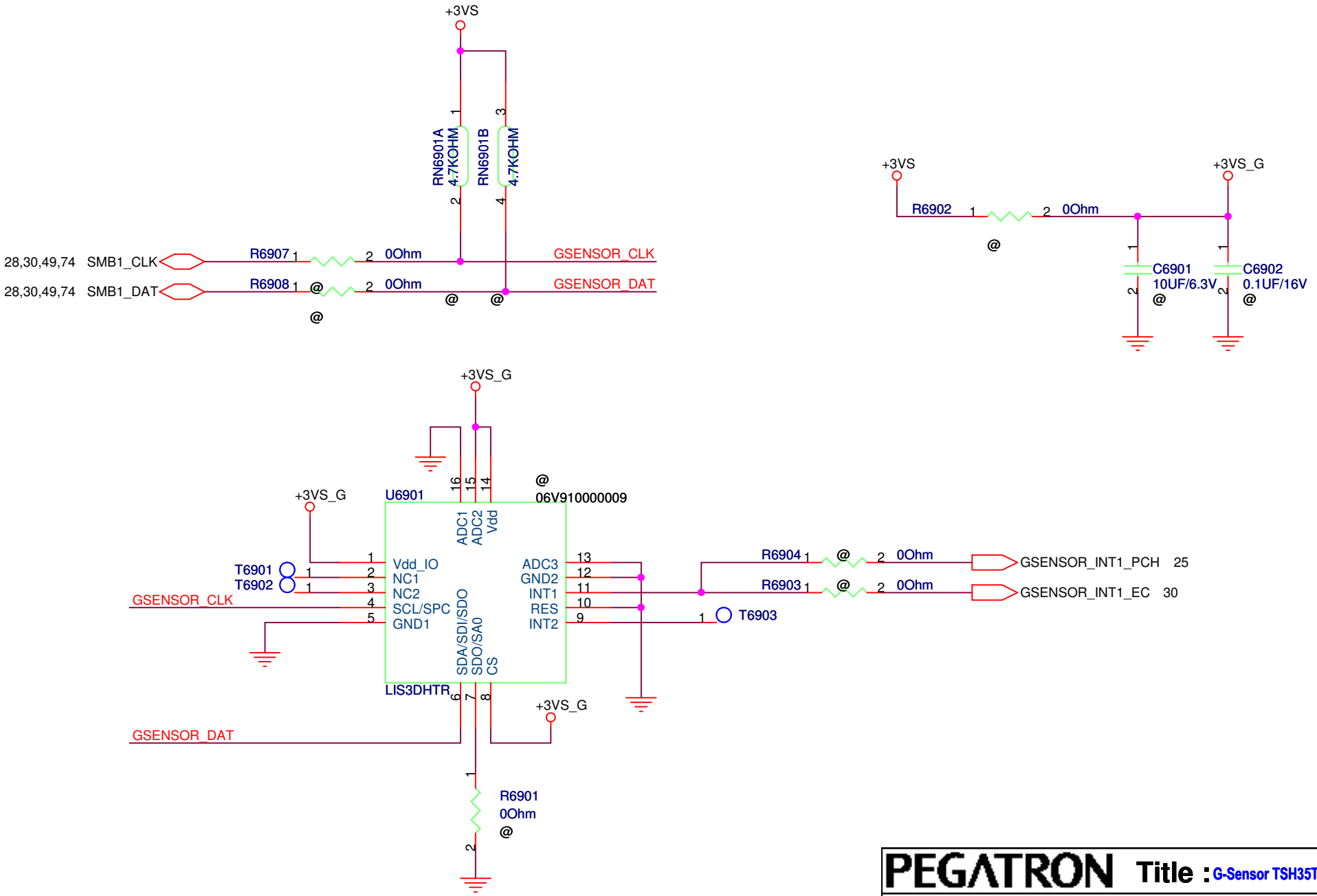
Title : Finger Printer

Pegatron Corp.

Engineer: *Wing_Cheng*

Size	Project Name	Rev
A	**BA52HR/CR**	1.0

Date: Friday, February 03, 2012 Sheet 68 of 77



PEGATRON

Title : G-Sensor TSH35TR

BU1-RD Div.1-HW RD Dept.1

Engineer: Wing_Cheng

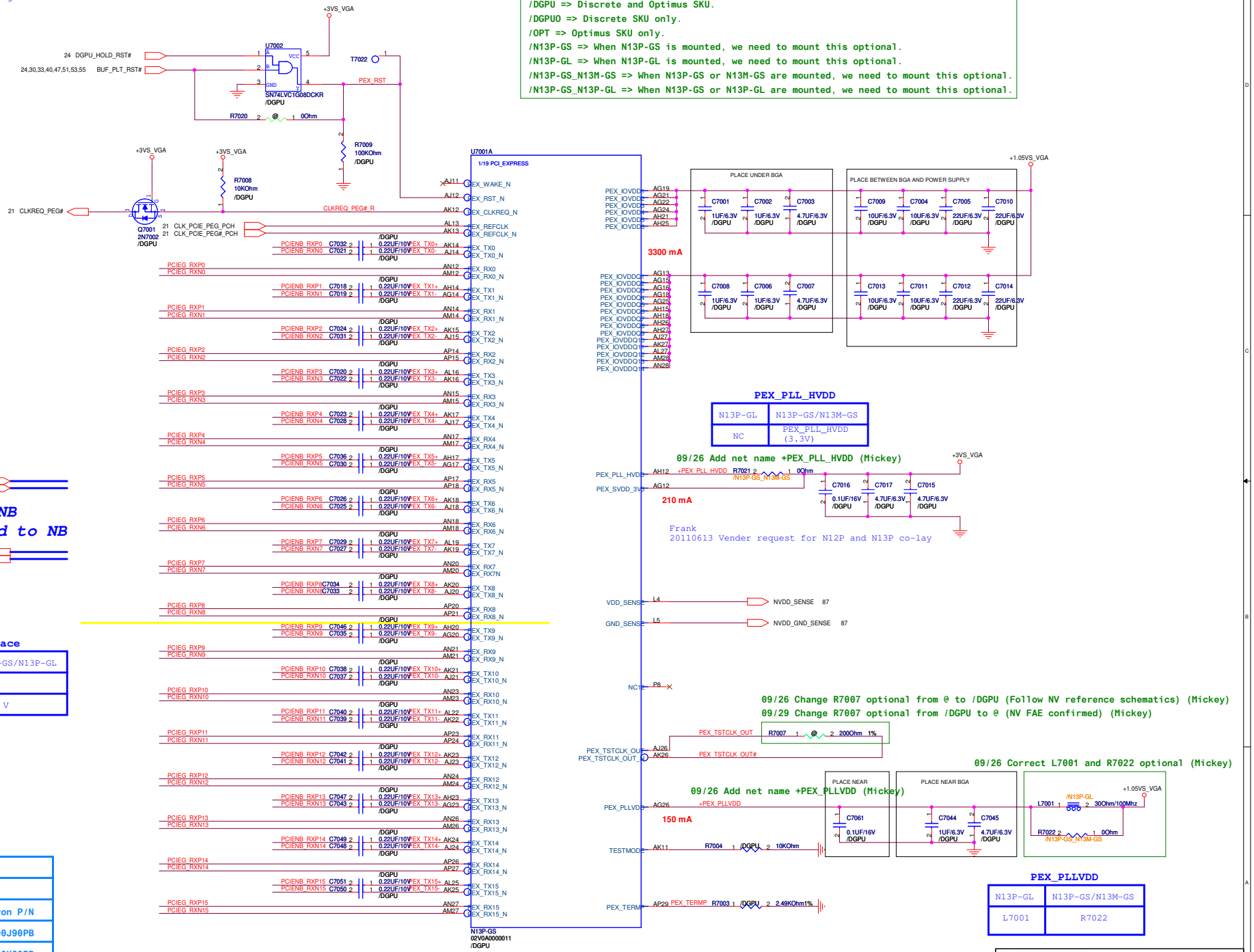
Size	Project Name	Rev
A		1.0

Date: Friday, February 03, 2012 Sheet 69 of 77

Frank
20110513 Change N13P GPU.

GPU BOM Optional Definition

@ => Unmount.
/DGPU => Discrete and Optimus SKU.
/DGPUO => Discrete SKU only.
/OPT => Optimus SKU only.
/N13P-GS => When N13P-GS is mounted, we need to mount this optional.
/N13P-GL => When N13P-GL is mounted, we need to mount this optional.
/N13P-GS_N13M-GS => When N13P-GS or N13M-GS are mounted, we need to mount this optional.
/N13P-GS_N13P-GL => When N13P-GS or N13P-GL are mounted, we need to mount this optional.



3 PCIENB_RXP[0..15]
3 PCIENB_RXN[0..15]

PEX=> From NB
EXP: VGA Card to NB

3 PCIEG_RXP[0..15]
3 PCIEG_RXN[0..15]

PEX_PLL_HVDD

N13P-GL	N13P-GS/N13M-GS
NC	PEX_PLL_HVDD (3.3V)

PCIE interface

	N13M-GS	N13P-GS/N13P-GL
8 Lane	V	
16 Lane		V

PEX_PLLVDD

N13P-GL	N13P-GS/N13M-GS
L7001	R7022

GPU Information		
GPU Location : U7001		
Type	Version	Pegatron P/N
N13P-GS	ES	020A-00J90PB
N13P-GL	QS	020A-00K60PB
N13M-GS	ES	020A-00JD0PB

PEGATRON
Title : GPU_PEG*16
PEGATRON COMPUTER INC
Engineer: Mickey_Yu
Size: C
Project Name: VA70_N13P-GDDR3
Rev: 1.0
P/N:
Date: Friday, February 03, 2012
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FB_CLAMP

N13P-GL	N13P-GS/N13M-GS
NC	PD 10K

FB_DLL_AVDD

N13P-GL	N13P-GS/N13M-GS
NC	FB_DLL_AVDD (1.05V)

FBB channel

	N13M-GS	N13P-GS/N13P-GL
FBB	X	V
FBA	V	V

09/26 Change R7120 optional from /DGPU to /N13P-GS_N13M-GS (Mickey)
09/27 Change net name from +FB_DLL_AVDD to +FB_PLL_AVDD (Mickey)

09/26 Add net name +FB_DLL_AVDD_R (Mickey)

11/14 Delete T7102,T7103,T7105,T7106,T7107,T7108 (NV Recommend) (Mickey)

09/26 Change R7103,R7104 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)

	N13M-GS	N13P-GS/N13P-GL
R7103/R7104	unmount	mount

09/26 Add net name +FB_PLL_AVDD_GPU (Mickey)
Frank
20110613 Vender request for N12P and N13P co-lay

FBB_PLL_AVDD

N13P-GL/N13M-GS	N13P-GS
NC	FBB_PLL_AVDD (1.05V)

Frank
20110613 Vender suggest C7119 change 22UF.

Title :	GPU_DDR3 FB	
PEGATRON COMPUTER INC	Engineer:	Mickey_Yu
Size: C	Project Name: VA70_N13P-GDDR3	Rev: 1.0
	P/N:	
Date: Friday, February 03, 2012	Sheet 71 of 99	

10/03 Change C7203 optional from /DGPUO to @ (Follow NV FAE recommend) (Mickey)
09/27 Change L7201 from 300ohm bead to 220ohm bead (Follow NV design guide) (Mickey)
09/27 Change R7202,C7206 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)
09/26 Change R7201 optional from /DGPU to /OPT (Mickey)
09/26 Change C7201~7205,L7201 optional from /DGPU to /DGPUO (Mickey)

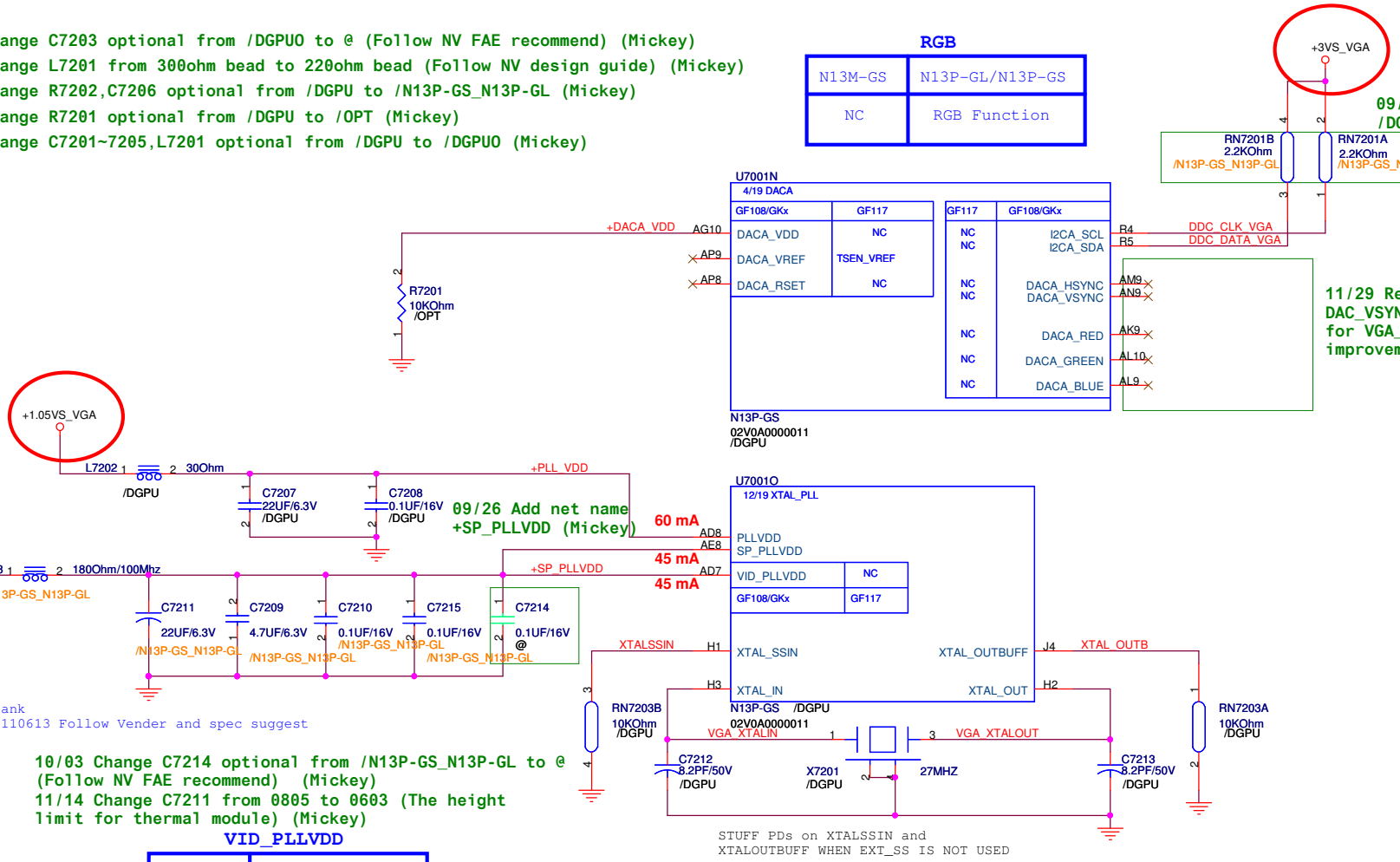
RGB

N13M-GS	N13P-GL/N13P-GS
NC	RGB Function

09/26 Change RN7201 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)

09/29 Correct the net name of DDC_CLK_VGA, DDC_DATA_VGA,DAC_HSYNC_VGA and DAC_VSYNC_VGA (Mickey)

11/29 Remove net DAC_HSYNC_VGA, DAC_VSYNC_VGA, DAC_VR, DAC_VG, DAC_VB for VGA_Vcore power plane improvement(Elmer)



Frank
20110613 Follow Vender and spec suggest

10/03 Change C7214 optional from /N13P-GS_N13P-GL to @ (Follow NV FAE recommend) (Mickey)
11/14 Change C7211 from 0805 to 0603 (The height limit for thermal module) (Mickey)

VID_PLLVDD

N13M-GS	N13P-GL/N13P-GS
NC	VID_PLLVDD (1.05V)

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

11/16 Change C7212,C7213 from 18pF to 8.2pF (Crystal vendor recommend) (Mickey)

PEGATRON
PEGATRON COMPUTER INC

Title : GPU_RGB/XTAL
Engineer: Mickey_Yu

Size	Project Name	Rev
B	VA70_N13P-GDDR3	1.0
	P/N	

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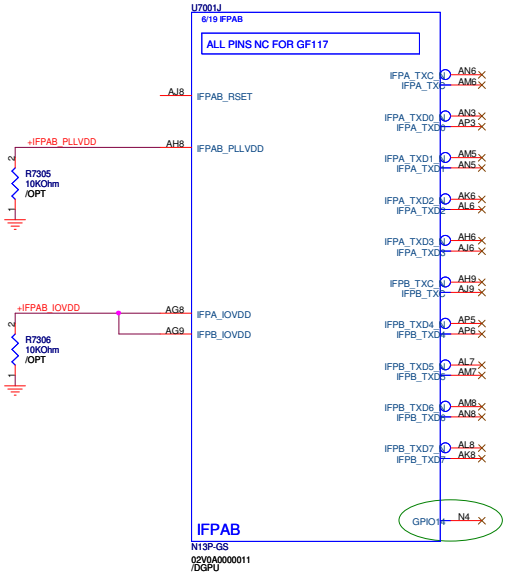
LVDS

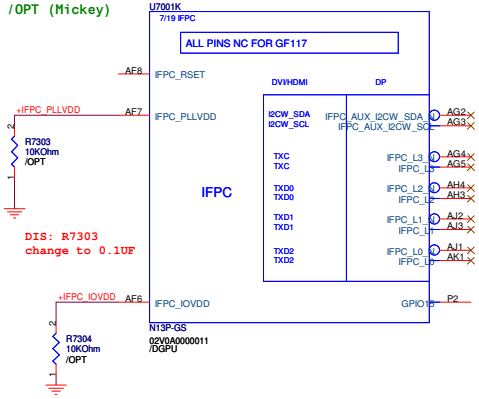


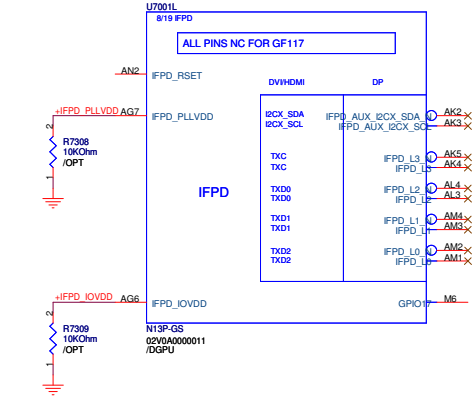
09/27 Change R7302 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)

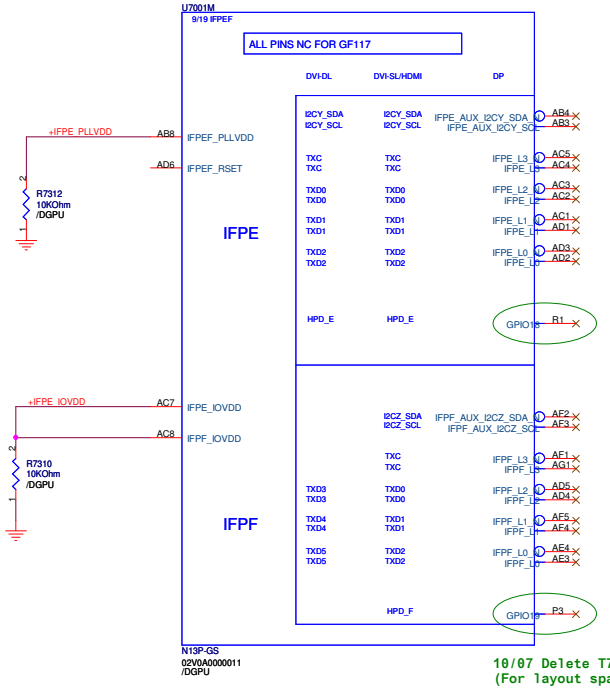
09/26 Change R7303,R7304 optional from /DGPU_ONLY to /OPT (Mickey)

09/26 Change C7307~7315,L7303,L7305 optional from /DGPU_ONLY to /DGPUO (Mickey)

HDMI







10/07 Delete T7310,T7311 (For layout spacing) (Mickey)

GPIO

	N13M-GS	N13P-GS/N13P-GL
GPIO14	X	V
GPIO15	X	V
GPIO16	X	V
GPIO17	X	V
GPIO18	X	V
GPIO19	X	V

IFPX channel

	N13M-GS	N13P-GS/N13P-GL	
IFPA/B	X	V	LVDS
IFPC	X	V	HDMI
IFPD	X	V	EDP
IFPE/F	X	V	

PEGATRON COMPUTER INC

Title : GPU_LVDS/HDMI/EDP

Engineer: Mickey_Yu

Size	Project Name	Rev
C	VA70_N13P-GDDR3	1.0
	P/N	

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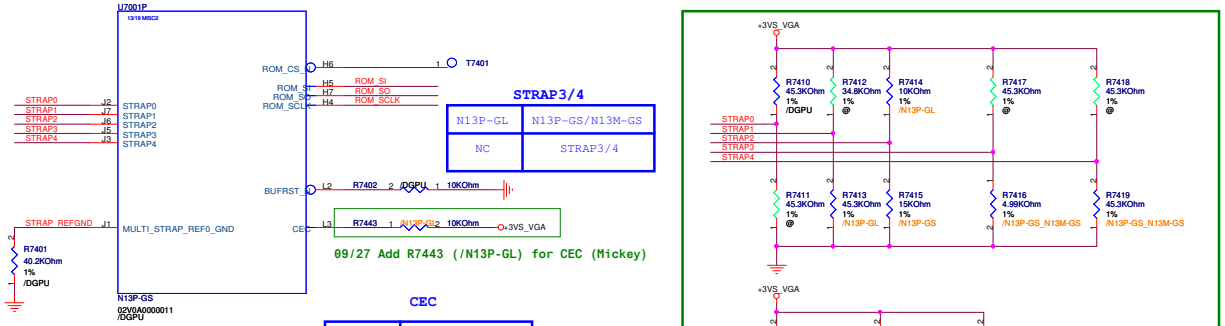


09/27 Add R7443 (/N13P-GL) for CEC (Mickey)

STRAP3/4

N13P-GL	N13P-GS/N13M-GS
NC	STRAP3/4

CEC

N13P-GL	N13P-GS/N13M-GS
PU 10K (3V3)	NC

N13P-GS ES2/QS

DEVICE ID	0xFDB		
STRAP0	45K PU		
STRAP1	35K PD		
STRAP2	15K PD		
STRAP3	5K PD		
STRAP4	10K PD		
ROM_SCLK	5K PU		
ROM_SI	Hynix 128Mx16	35K PD	
	Hynix 64Mx16	15K PD	R7407
ROM_SO	10K PU		

N13P-GL QS

DEVICE ID	0xDE9		
STRAP0	45K PU		
STRAP1	45K PD		
STRAP2	10K PU		R7414
STRAP3	NC		
STRAP4	NC		
ROM_SCLK	15K PD		
ROM_SI	Hynix 128Mx16	35K PD	
	Hynix 64Mx16	15K PD	R7407
ROM_SO	10K PU		

STRAP2--GPU TYPE

N13M-GS	N13P-GL	N13P-GS

ROM_SI--VRAM TYPE

HYNIX		SAMSUNG	
64Mx16	128Mx16	64Mx16	128Mx16

STRAP1 R7413	N13P-GS ES2/QS	N13P-GL QS
	35K	45K

ROM_SI R7407	Hynix 128Mx16	Hynix 64Mx16
	35K	15K

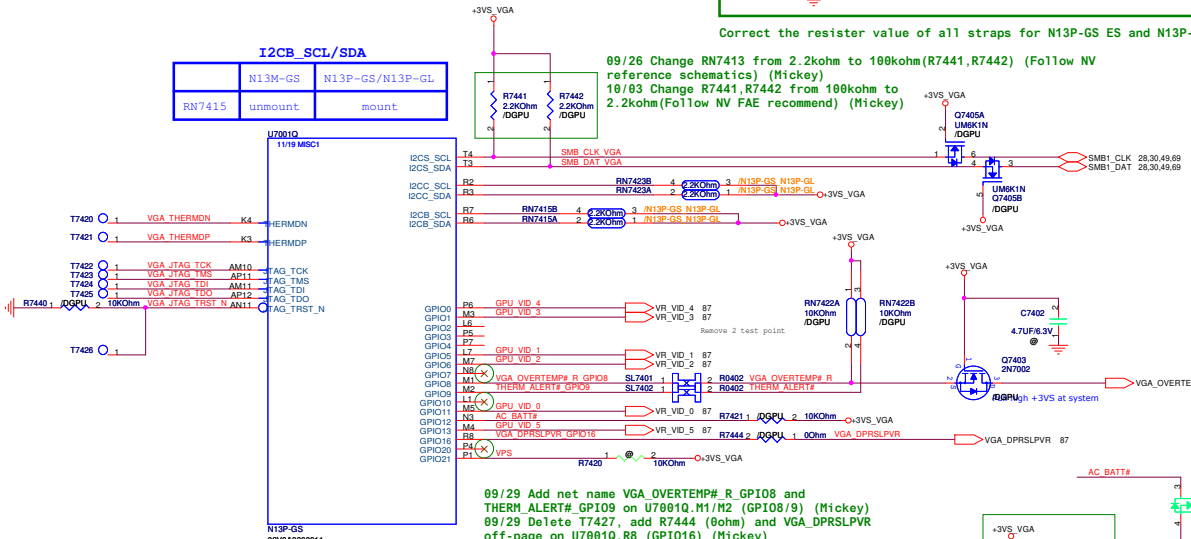
Correct the resister value of all straps for N13P-GS ES and N13P-GL QS (Follow NV FAE recommend)

11/28 Change R7413 from /DGPU to /N13P-GS (Follow NV FAE recommend) (Mickey)
11/28 Change R7414 from 20kohm to 10kohm(/N13P-GL) (Follow NV FAE recommend) (Mickey)
11/28 Change R7415 from 5kohm to 15kohm(/N13P-GS) (Follow NV FAE recommend) (Mickey)

I2CB_SCL/SDA

	N13M-GS	N13P-GS/N13P-GL
RN7415	unmount	mount

09/26 Change RN7413 from 2.2kohm to 100kohm(R7441,R7442) (Follow NV reference schematics) (Mickey)
10/03 Change R7441,R7442 from 100kohm to 2.2kohm(Follow NV FAE recommend) (Mickey)



09/29 Add net name VGA_OVERTEMP#_R_GPIO8 and THERM_ALERT#_GPIO9 on U7001Q.M1/M2 (GPIO8/9) (Mickey)
09/29 Delete T7427, add R7444 (0ohm) and VGA_DPRSLPVR off-page on U7001Q.R8 (GPIO16) (Mickey)
10/07 Delete T7428,T7433,T7435 (For layout spacing) (Mickey)

GPIO

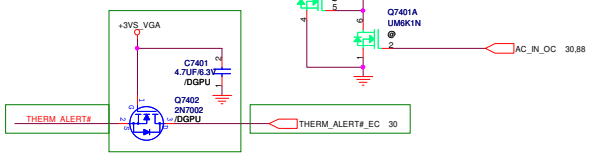
	N13M-GS	N13P-GS/N13P-GL
GPIO20	X	X
GPIO21	X	X

GPIO 8

	N13P-GL	N13P-GS/N13M-GS
Q7403	unmount	NV suggestion mount

N13P-GT ES2/QS

DEVICE ID	0xFD1		
STRAP0	45K PU		
STRAP1	35K PD		
STRAP2	10K PD		
STRAP3	5K PD		
STRAP4	10K PD		
ROM_SCLK	5K PU		
ROM_SI	Hynix 128Mx16	35K PD	
	Hynix 64Mx16	15K PD	R7407
ROM_SO	10K PU		



09/29 Change Q7401,Q7402 optional from @ to /DGPU(Mickey)
09/29 Change net name from VPS to THERM_ALERT# on Q7402.2 (Mickey)
09/29 Change net name from VPS_EC to THERM_ALERT#_EC on Q7402.3 (Mickey)

PEGATRON

Title : GPU_GPIO/STRAP

PEGATRON COMPUTER INC

Engineer: Mickey_Yu

Size	Project Name	Rev
A2	VA70_N13P-GDDR3	1.0
	P/N	

Date: Friday, February 03, 2012 Sheet 74 of 89

09/26 Add net name +VDD33_GPU (Mickey)

09/26 Add C7506,C7508,C7509 (Follow NV reference schematics) (Mickey)

09/27 Remove C7506,C7508,C7509 (Follow NV design guide) (Mickey)

+VGA_VCORE

U7001E

14/19 NVVDD

PLACE UNDER GPU

C7511 C7510 C7513 C7512 C7515 C7514 C7517 C7516 0.1UF/16V /DGPU

C7518 C7519 C7520 C7521 C7522 C7523 C7524 C7530 4.7UF/6.3V /DGPU

C7525 C7526 C7527 C7528 C7529 C7536 C7537 4.7UF/6.3V /DGPU

CE7501 330UF/2V /DGPU 1BV080000010

C7531 C7532 C7533 C7534 C7535 4.7UF/6.3V /DGPU

C7552 22UF/6.3V /DGPU

C7553 47UF/4V @

PLACE NEAR GPU

GND

N13P-GS

02V0A0000011

/DGPU

09/29 Change C7518~C7537 from 10uF to 4.7uF (Follow NV design guide) (Mickey)

U7001F

18/19 NC/VDD33

AC6 AJ28 AJ4 AJ5 AL11 C15 D19 D20 D23 D26 H31 T8 V32

NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC13 NC14

VDD33_1 VDD33_2 VDD33_3 VDD33_4

J8 K8 L8 M8

+VDD33_GPU

C7507 C7501 C7504 C7505 0.1UF/16V /DGPU

PLACE NEAR BALLS

C7502 1UF/6.3V /DGPU

C7503 4.7UF/6.3V /DGPU

PLACE NEAR BGA

GND

+3VS_VGA

R7501 0OHm /DGPU

N13P-GS

02V0A0000011

/DGPU

VDD33

N13P-GS	N13P-GL/N13M-GS
3V3MISC isolation circuitry	VDD33

check with NV==>可先不用Isolation circuitry

Frank

20110613 Follow Vender and spec suggest

=> Add C7542, C7543, C7544, C7545 and C7556 mount

Remove C7540, C7561, C7558, C7649

Change C7541, C7557 to 10uF

+1.5VS_VGA

U7001D

15/19 FBVDDQ

AA27 AA30 AB27 AB33 AC27 AD27 AE27 AF27 AG27 B13 B16 B19 E13 E16 E19 H10 H11 H12 H13 H14 H15 H16 H18 H19 H20 H21 H22 H23 H24 H6 H9 L27 M27 N27 P27 R27 T27 T30 T33 V27 W27 W30 W33 Y27

FBVDDQ1 FBVDDQ2 FBVDDQ3 FBVDDQ4 FBVDDQ5 FBVDDQ6 FBVDDQ7 FBVDDQ8 FBVDDQ9 FBVDDQ10 FBVDDQ11 FBVDDQ12 FBVDDQ13 FBVDDQ14 FBVDDQ15 FBVDDQ16 FBVDDQ17 FBVDDQ18 FBVDDQ19 FBVDDQ20 FBVDDQ21 FBVDDQ22 FBVDDQ23 FBVDDQ24 FBVDDQ25 FBVDDQ26 FBVDDQ27 FBVDDQ28 FBVDDQ29 FBVDDQ30 FBVDDQ31 FBVDDQ32 FBVDDQ33 FBVDDQ34 FBVDDQ35 FBVDDQ36 FBVDDQ37 FBVDDQ38 FBVDDQ39 FBVDDQ40 FBVDDQ41 FBVDDQ42 FBVDDQ43 FBVDDQ44

C7539 C7559 C7542 C7544 C7538 C7555 C7554 C7541 0.1UF/16V /DGPU

1UF/6.3V /DGPU

4.7UF/6.3V /DGPU

10UF/6.3V /DGPU

C7551 C7556 C7543 C7545 C7560 C7562 C7550 C7557 0.1UF/16V /DGPU

C7563 C7564 C7565 @ 0.1UF/16V

11/21 Add C7563,C7564,C7565 (0.1uF) at +1.5VS_VGA (EMI Recommend) (Mickey)

CALIBRATION PIN	GDDR5
FB_CALx_PD_VDDQ	40
FB_CALx_PU_GND	40
FB_CALx_TERM_GND	60

FB_VDDQ_SENSE F1 FBVDDQ_SENSE T7508

FB_GND_SENSE F2 FBVDDQ_GND_SENSE T7509

FB_CAL_PD_VDDQ J27 +FB_CAL_PD_VDDQ R7507 /DGPU 40.2Ohm 1%

FB_CAL_PU_GND H27 +FB_CAL_PU_GND R7509 /DGPU 42.2Ohm 1%

FB_CAL_TERM_GND H25 +FB_CAL_TERM_GND R7510 /DGPU 51.1Ohm 1%

PLACE CLOSE TO GPU BALLS

+1.5VS_VGA

GND

N13P-GS

02V0A0000011

/DGPU

09/28 Change R7510 from 60.4ohm to 51.1ohm (Follow NV design guide) (Mickey)

Frank

20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm

U7001G

18/19 GND_1/2

A2 AA17 AA18 AA20 AA22 AB12 AB14 AB16 AB19 AB2 AB21 A33 AB23 AB28 AB30 AB32 AB5 AB7 AC13 AC15 AC17 AC18 AA13 AC20 AC22 AE2 AE28 AE30 AE32 AE33 AE5 AE7 AH10 AA15 AH13 AH16 AH19 AH2 AH22 AH24 AH28 AH29 AH30 AH32 AH33 AH5 AH7 AJ7 AK10 AK7 AL12 AL14 AL15 AL17 AL18 AL2 AL20 AL21 AL23 AL24 AL26 AL28 AL30 AL32 AL33 AL5 AM13 AM16 AM19 AM22

GND1 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND2 GND15 GND16 GND17 GND18 GND19 GND20 GND21 GND22 GND23 GND24 GND3 GND25 GND26 GND27 GND28 GND29 GND30 GND31 GND32 GND33 GND35 GND4 GND37 GND38 GND39 GND40 GND41 GND42 GND43 GND44 GND45 GND46 GND47 GND48 GND49 GND50 GND51 GND52 GND53 GND54 GND55 GND56 GND57 GND58 GND59 GND60 GND61 GND62 GND63 GND64 GND65 GND66 GND67 GND68 GND69 GND70 GND71 GND72

GND73 GND74 GND75 GND76 GND77 GND78 GND79 GND80 GND81 GND82 GND83 GND84 GND85 GND86 GND87 GND88 GND89 GND90 GND91 GND92 GND93 GND94 GND95 GND96 GND97 GND98 GND99 GND100 GND101 GND102 GND103 GND104 GND105 GND106 GND107 GND108 GND109 GND110 GND111 GND112 GND113 GND114 GND115 GND116 GND117 GND118 GND119 GND120 GND121 GND122 GND123 GND124 GND125 GND126 GND127 GND128 GND129 GND130 GND131 GND132 GND133 GND134 GND135 GND136 GND137 GND138 GND139 GND140 GND141 GND142

AM25 AN1 AN10 AN13 AN16 AN19 AN22 AN25 AN30 AN34 AN4 AN7 AP2 AP33 B1 B10 B22 B25 B28 B31 B34 B4 B7 C10 C13 C19 C22 C25 C28 C7 D2 D31 D33 E10 E22 E25 E5 E7 F28 F7 G10 G13 G16 G19 G2 G22 G25 G28 G3 G30 G32 G33 G5 G7 K2 K28 K30 K32 K33 K5 K7 M13 M15 M17 M18 M20 M22 N12 N14 N16

N13P-GS

02V0A0000011

/DGPU

U7001I

17/19 GND_2/2

N19 N2 N21 N23 N28 N30 N32 N33 N5 N7 P13 P15 P17 P18 P20 P22 R12 R14 R16 R19 R21 R23 T13 T15 T17 T18 T2 T20 T22

GND143 GND144 GND145 GND146 GND147 GND148 GND149 GND150 GND151 GND152 GND153 GND154 GND155 GND156 GND157 GND158 GND159 GND160 GND161 GND162 GND163 GND164 GND165 GND166 GND167 GND168 GND169 GND170 GND171

GND172 GND173 GND174 GND175 GND176 GND177 GND178 GND179 GND180 GND181 GND182 GND183 GND184 GND185 GND186 GND187 GND188 GND189 GND190 GND191 GND192 GND193 GND194 GND195 GND196 GND197 GND198 GND199 GND200

T28 T32 T5 T7 U12 U14 U16 U19 U21 U23 V12 V14 V16 V19 V21 V23 W13 W15 W17 W18 W20 W22 W28 Y12 Y14 Y16 Y19 Y21 Y23

AG11 GND34 GND36 AH11

GND_OPT1 GND_OPT2 C16 W32

Optional GND GNDs (2)

NC for 4-Lyr cards

N13P-GS

02V0A0000011

/DGPU

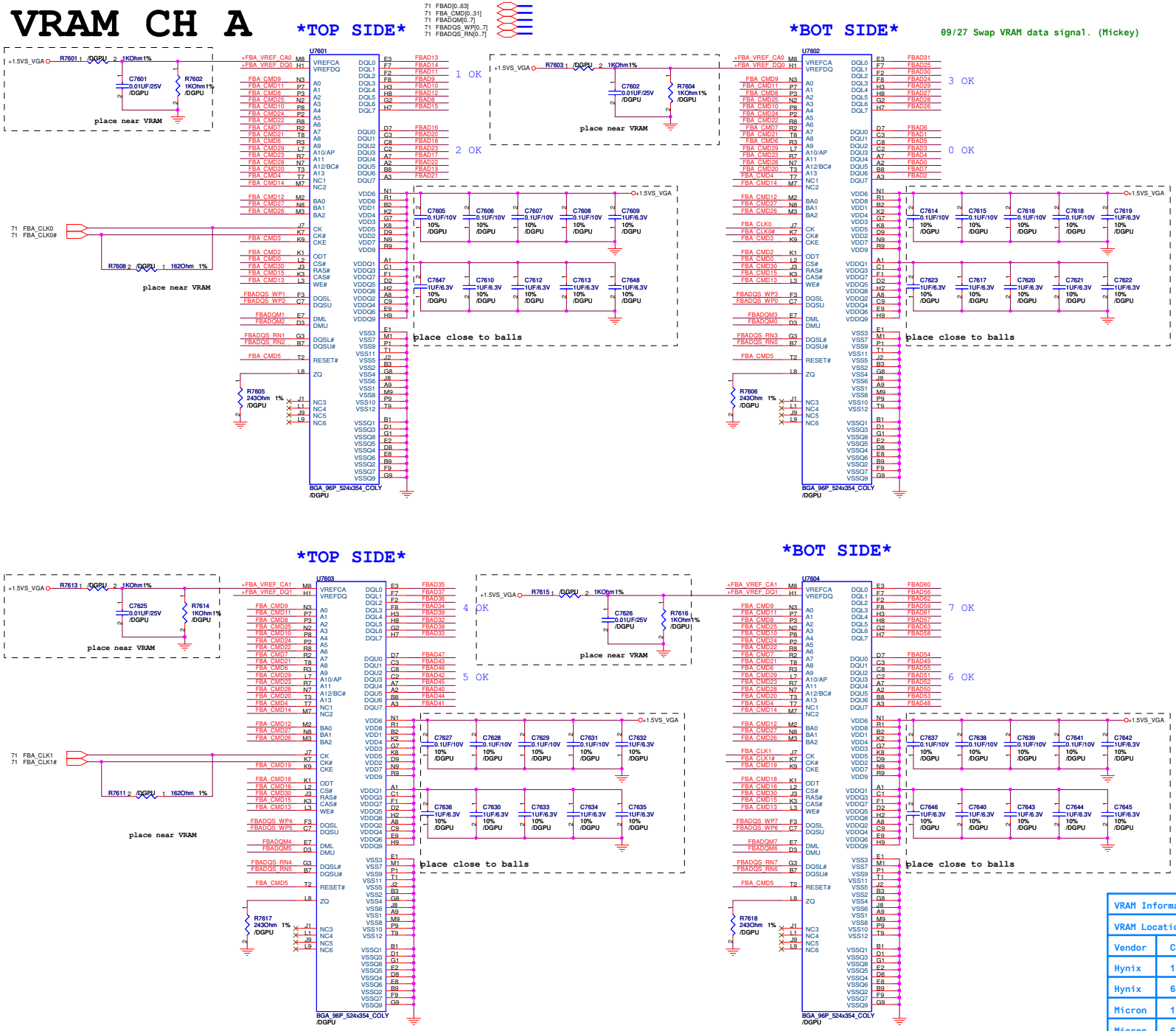
GND

VRAM CH A

TOP SIDE

BOT SIDE

09/27 Swap VRAM data signal. (Mickey)



M13X DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		

VRAM Information				VRAM Strap	
VRAM Location : U7601,U7602,U7603,U7604,U7701,U7702,U7703,U7704				VRAM Strap Location : R7407	
Vendor	Configuration	Pegatron P/N	Manufacturer P/N		
Hynix	128Mx16	0315-00ND0PB	H5TQ2G63BFR-11C	0x6	35K
Hynix	64Mx16	0315-00NF0PB	H5TQ1G63DFR-11C	0x2	15K
Micron	128Mx16	TBD	MT41J128M16JT-107G:K	TBD	TBD
Micron	64Mx16	0315-00SG0PB	MT41J64M16JT-107G:G	TBD	TBD

PEGATRON COMPUTER INC

Title : GPU_VRAM CHA

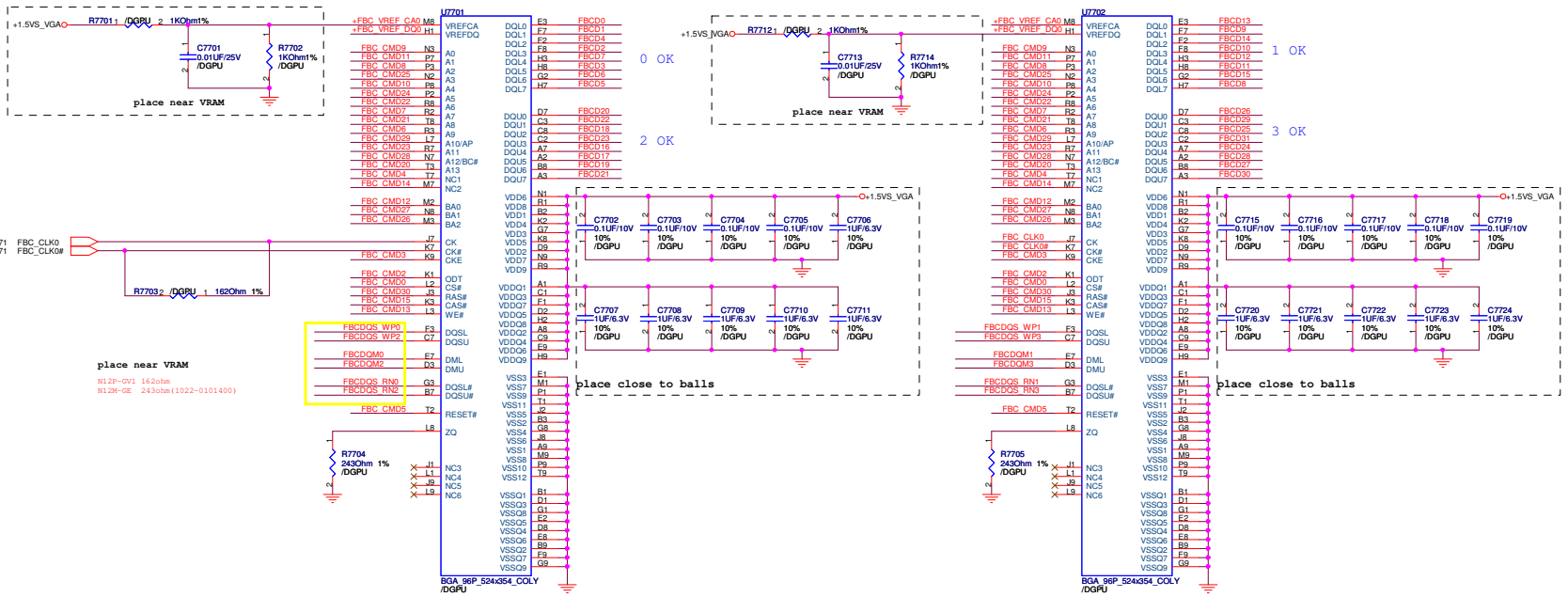
Engineer: Mickey_Yu

Size	Project Name	Rev
A2	VA70 N13P-GDDR3	1.0
	P/N	

Date: Friday, February 03, 2012 Sheet 78 of 99

VRAM CH C

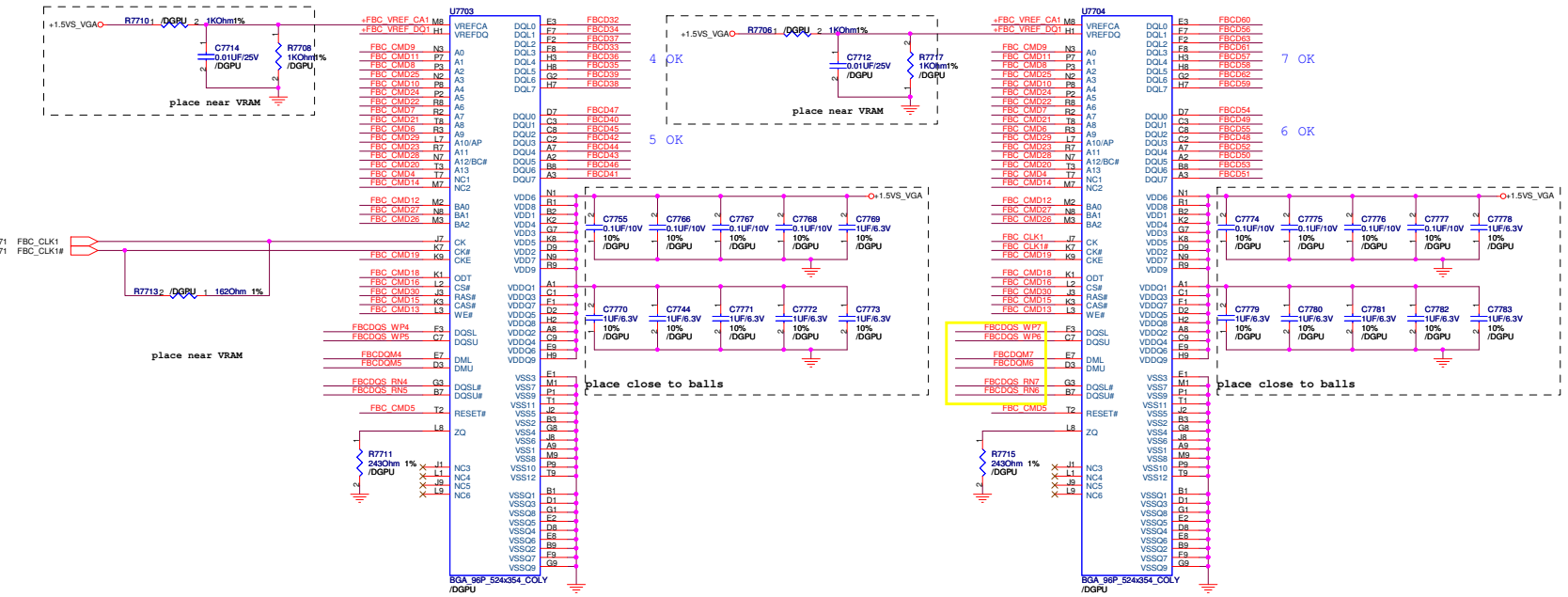
TOP SIDE



BOT SIDE

09/27 Swap VRAM data signal. (Mickey)

TOP SIDE



BOT SIDE

M13X DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		

PEGATRON COMPUTER INC

Title : GPU_VRAM CHB

Engineer: Mickey_Yu

Size: Custom | Project Name: VA70_N13P-GDDR3 | Rev: 1.0

P/N:

Date: Friday, February 03, 2012 | Sheet 77 of 99

PEGATRON

Title :

PEGATRON COMPUTER INC

Engineer: Mickey_Yu

Size	Project Name	Rev
C	VA70_N13P-GDDR3	1.0
	P/N	

Date: Friday, February 03, 2012 Sheet 78 of 99

PEGATRON	Title : GPU_PEG*16		
PEGATRON COMPUTER INC	Engineer: Mickey_Yu		
Size: C	Project Name: VA70_N13P-GDDR3		Rev: 1.0
	P/N:		
Date: Friday, February 03, 2012	Sheet 79 of 99		

@=UMMOUNT
Schematic for Quad core use

Icc_TDC: Icc_Max
SV-QC 52A SV-QC 94A
SV-DC 36A SV-DC 53A

Switching Frequency=300KHz
ICC MAX=45A

Vboot=0V
ICC MAX=94A

For ATS Vboot=1.1 Short T80131 To Ground

Icc_TDC: Icc_MAX:
QC 38A QC 46A
SV-DC 21.5A SV-DC 33A

For Quad Core(GT2):
1.Remove DC_@ (R8021,R8051,C8055,C8022,C8044)

For Dual Core:
1.Remove QC_@, Add (R8021,R8051,C8055,C8022,C8044)
2.Change R8084 to 499ohm(10V2200000076),(OCP>60A)
3.Change R8085 to 2.37Kohm,(10V2200000044),Load line=1.86
4.Change R8034 to 499ohm,(10V2200000076),OCP>37A
5.Change R8042 to 3Kohm(10V2200000232),Load line=3.9
6.Change R8048 to 20Kohm(10V2200000036),ICC MAX=53A
7.Change R8045 to 154Kohm(10V2200000259),ICC MAX=33A,Switching Freq.=300KHz
8.Change C8023 to 0.1uf/25v(1AV300000007)

For Common BOM, Remove @

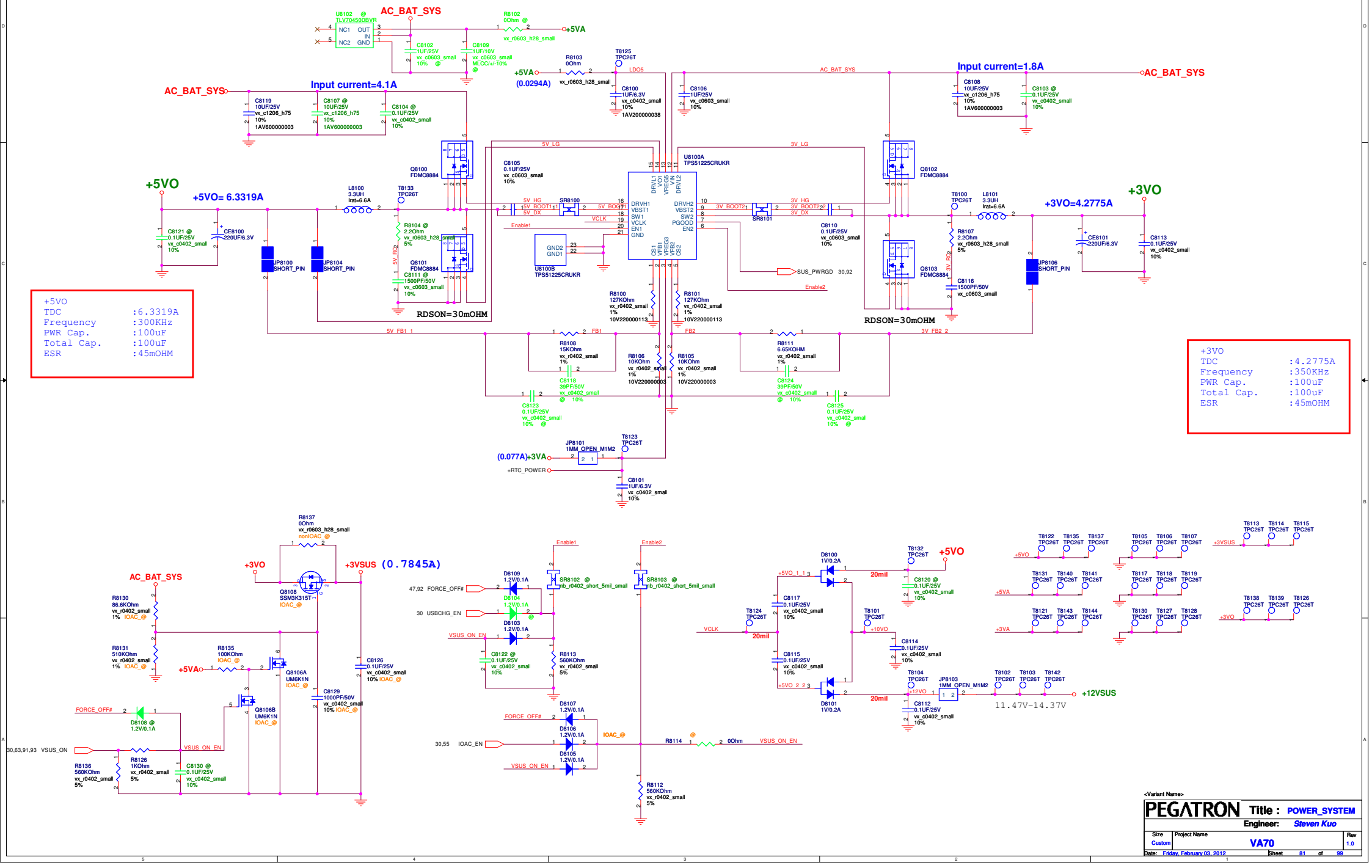
For UMA SKU
Remove @ and DSC_@

For DSC SKU
Remove @

<variant_name>

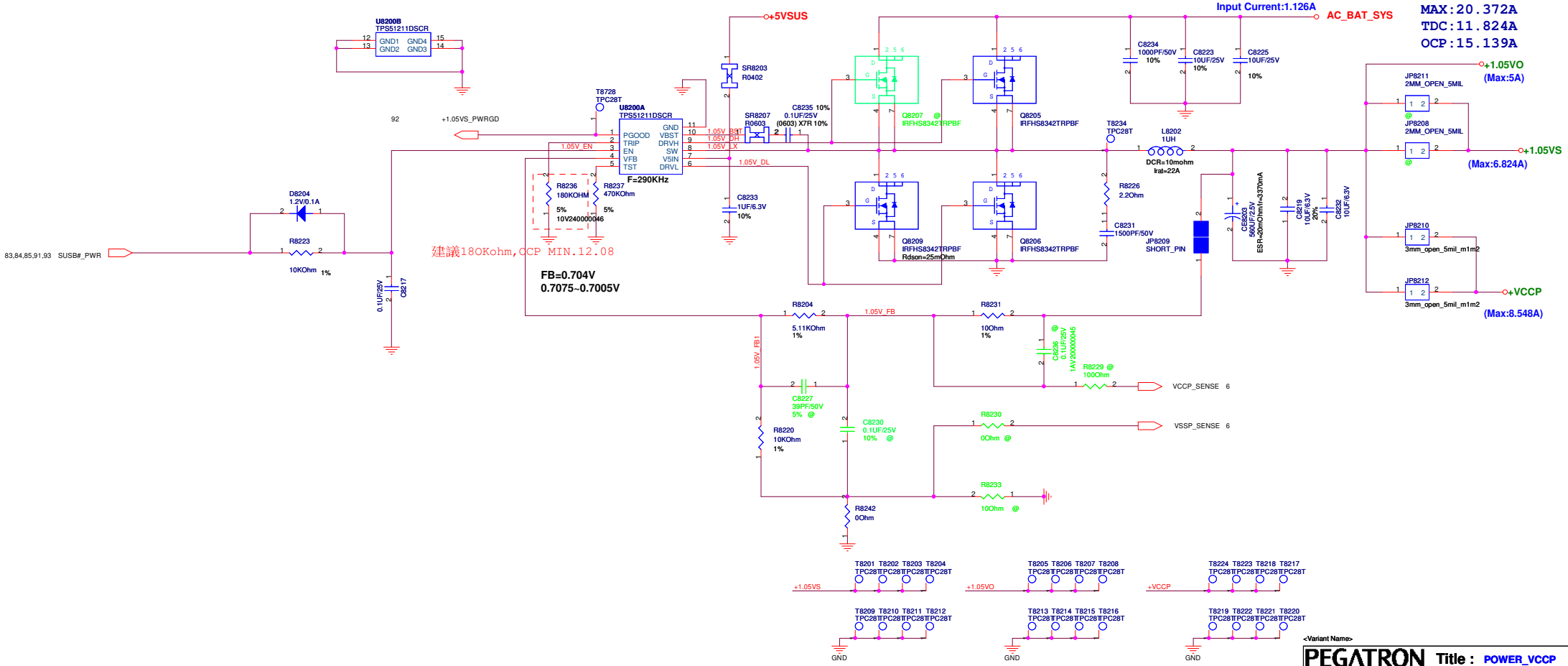
PEGATRON Title : POWER_VCORE
Engineer: Steven Kuo
Size: Custom | Project Name: VA70 | Rev: 1.1
Date: Friday, February 03, 2012 | Sheet 80 of 94

+5VO & +3VO POWER SUPPLY

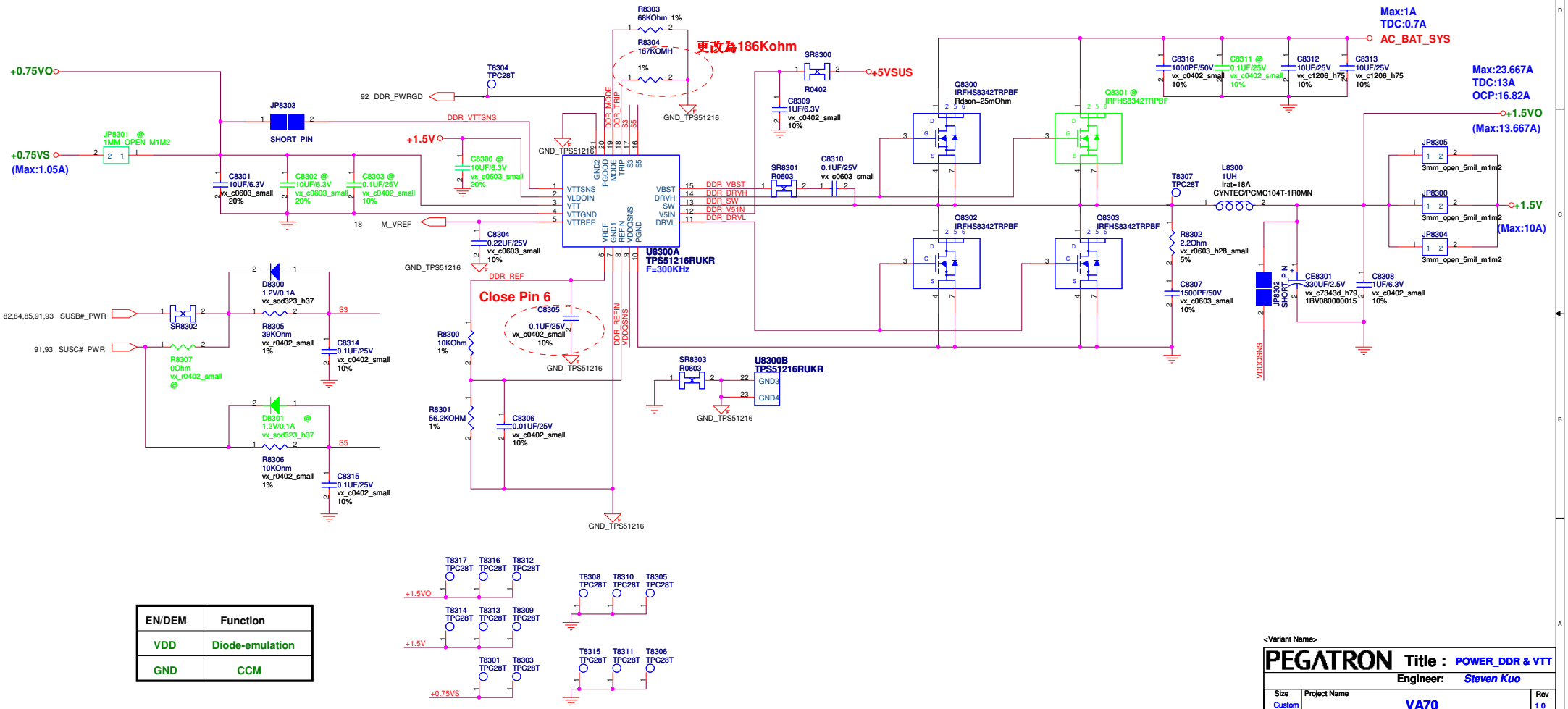


TRIP V (mV) = TRIP R (k) * TRIP I (mA)
TRIPI current, which is 10uA
VOCP = TRIP V / (8 / Rdson) + (I ripple / 2)

Used for testing purpose in production line.
Pull down to GND with a resistor of 470 kΩ or less



DDR & VTT POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

<Variant Name>

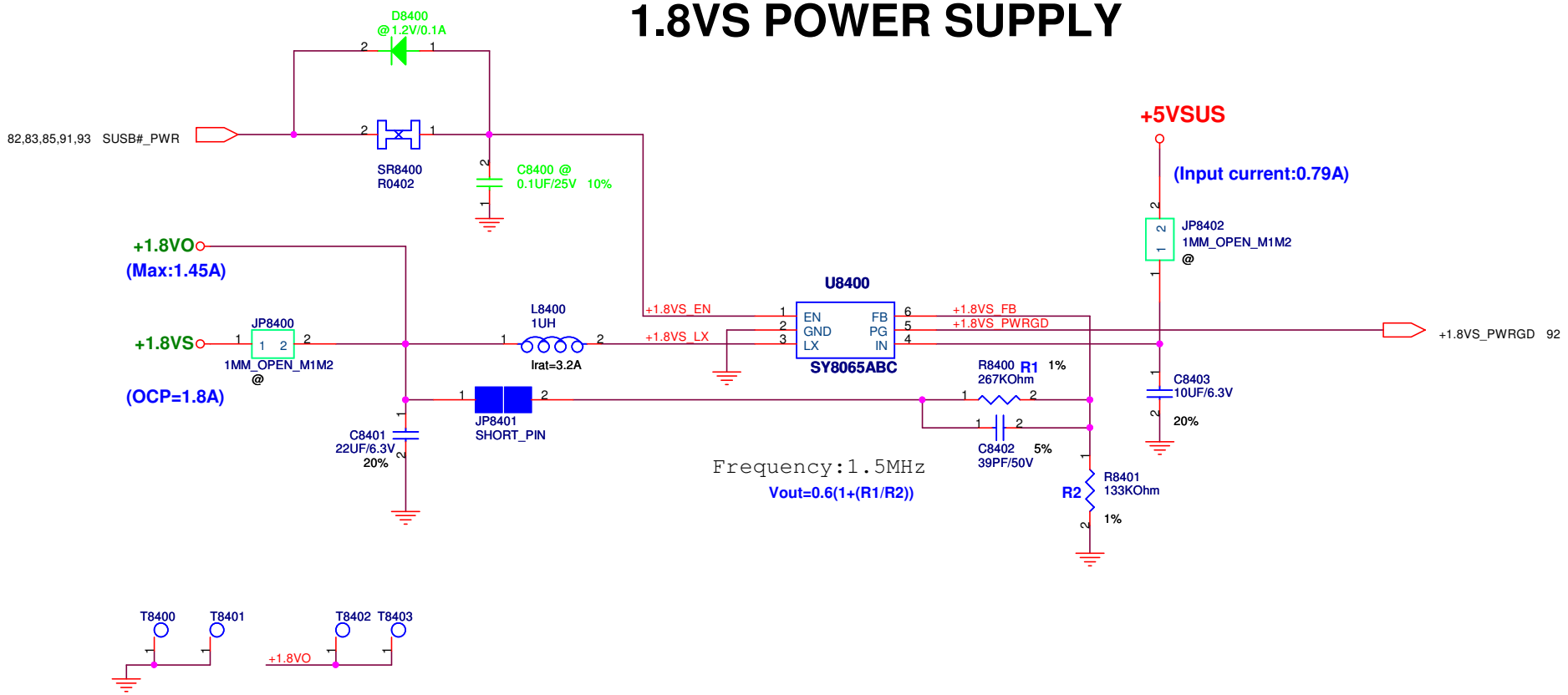
PEGATRON Title : POWER_DDR & VTT

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

Date: Friday, February 03, 2012 Sheet 83 of 94

1.8VS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_1.8VS

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

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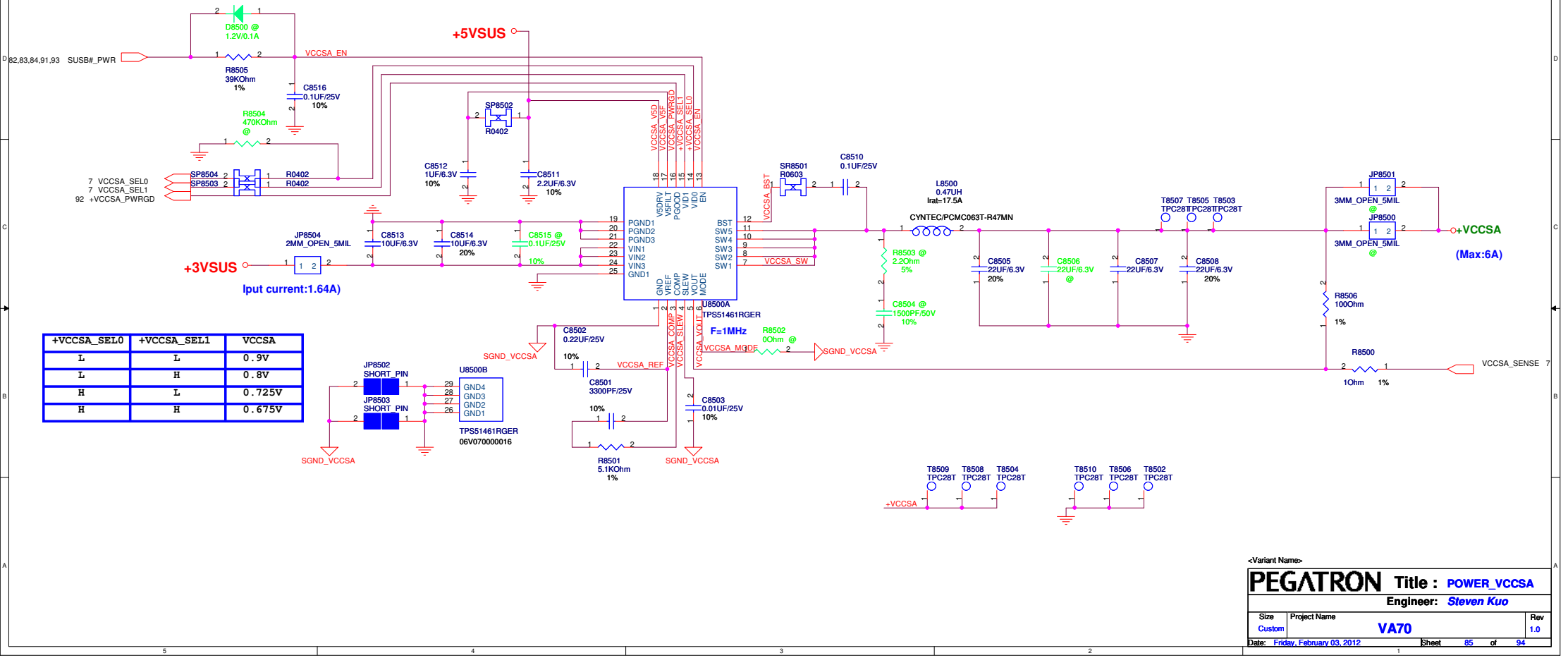
VCCSA POWER SUPPLY



+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Variant Name>

PEGATRON Title : POWER_VCCSA

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

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<Variant Name>

PEGATRON

Title : POWER_

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

Date: Friday, February 03, 2012 Sheet 86 of 94

VGA_CORE POWER SUPPLY

VID Set 0.9V

VGA_DPRSLPVR	VGA_PSI#	VO_action
L	L	1 Phase CCM
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

OCP : 60A

EDP=50A

+VGA_VCORE_O

+VGA_VCORE

AC_BAT_SYS

VID Set

+3VS_VGA

+1.05VS

+5VS

+VGA_VCORE

U8700A ISL62882CHRTZ-T

U8700B ISL62882CHRTZ-T

Q8701 RMW150N03FUB

Q8710 RMW150N03FUB

Q8709 RMW200N03FUB

Q8702 RMW200N03FUB

Q8703 RMW150N03FUB

Q8708 RMW150N03FUB

Q8704 RMW200N03FUB

Q8707 RMW200N03FUB

L8702 0.36UH Irat=60A DCR = 1.3m OHM

L8701 0.36UH Irat=60A DCR = 1.3m OHM

JP8706 SHORT_PIN

JP8702 SHORT_PIN

JP8705 SHORT_PIN

JP8701 SHORT_PIN

JP8703 SHORT_PIN

R8703=(Period(us)-0.29)*2.65

Period(us)=1/300KHz

R8706 Setting OCP

<Variant Name>

PEGATRON Title : POWER_VGACORE

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.2

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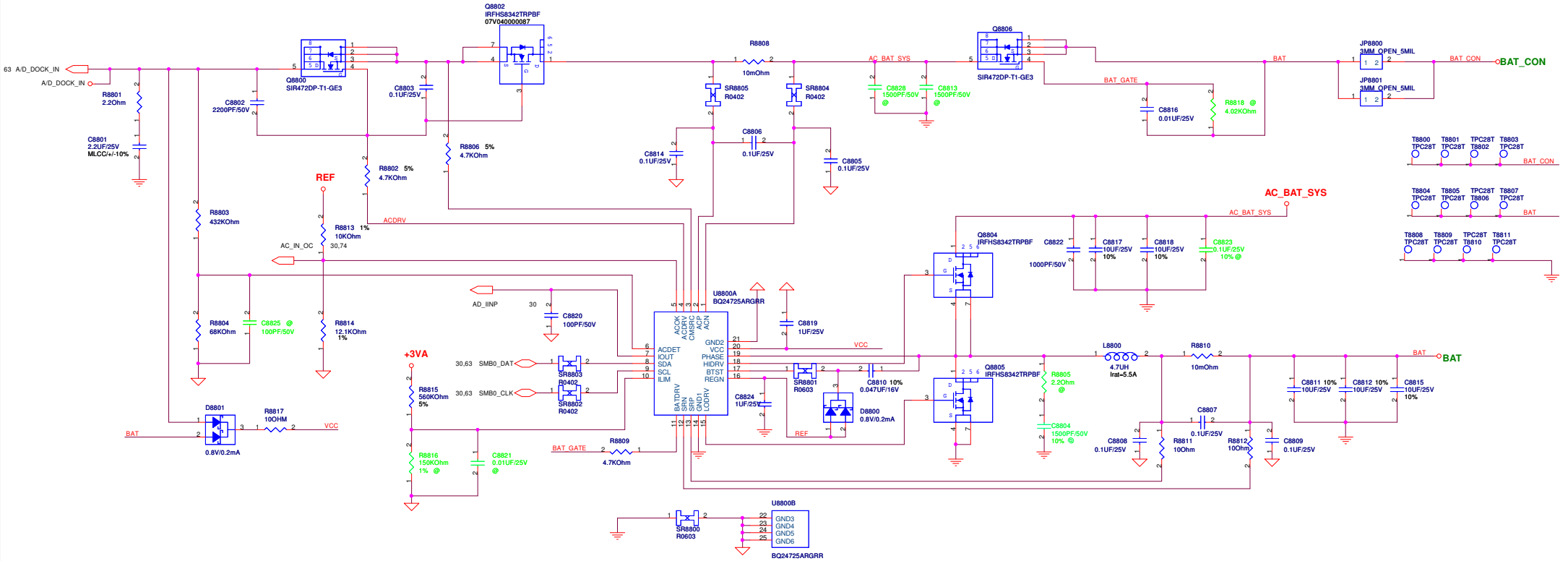
BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

Date: Friday, February 03, 2012 Sheet 88 of 15

<Variant Name>

PEGATRON Title : POWER_N/A

Engineer:

Size	Project Name	Rev
A		1.1

Date: Friday, February 03, 2012 Sheet 89 of 99

BATTERY IN DETECT

<Variant Name>

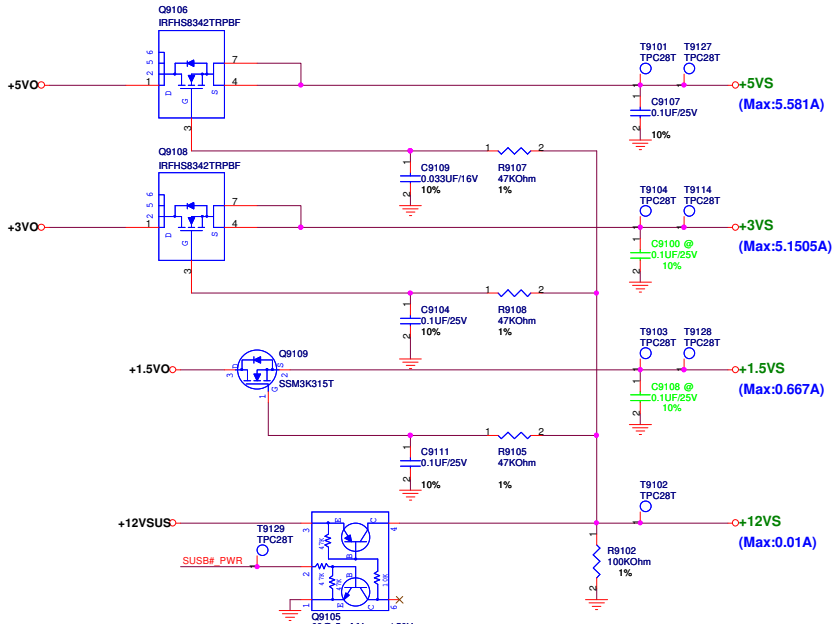
PEGATRON Title : POWER_DETECT

Engineer: *Steven Kuo*

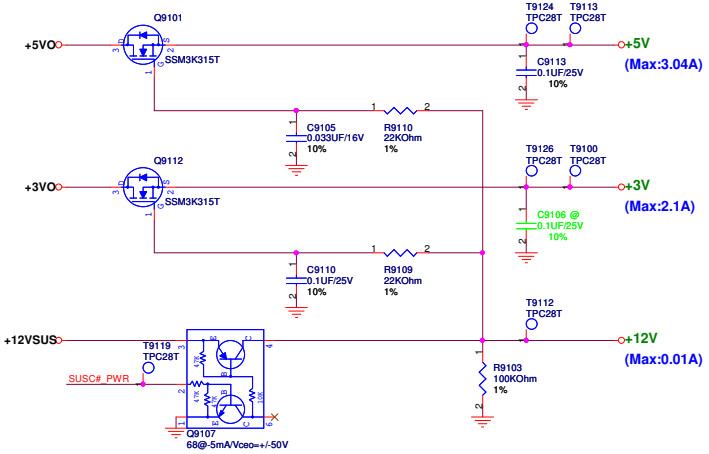
Size	Project Name	Rev
Custom	VA70	1.0

Date: Friday, February 03, 2012 Sheet 90 of 99

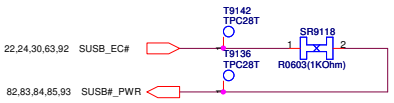
SUSB#_PWR POWER



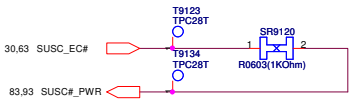
SUSC#_PWR POWER



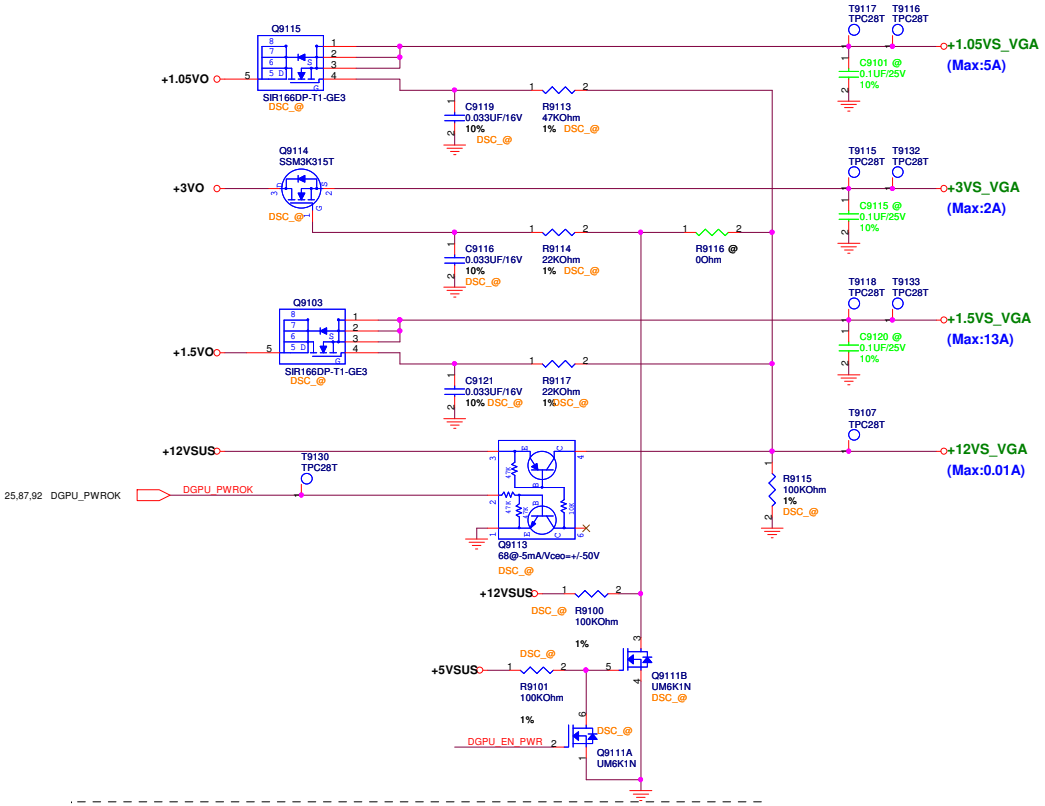
SUSB#_PWR POWER Control



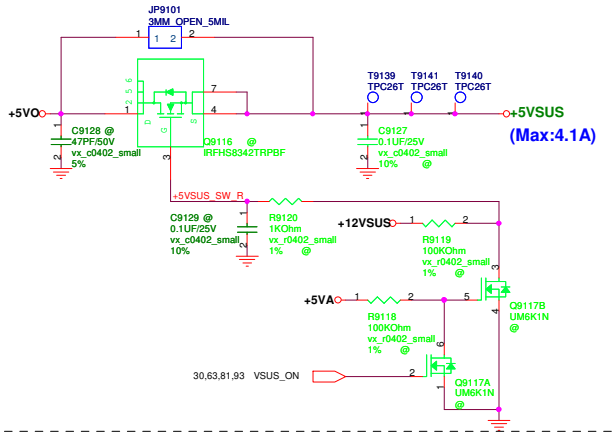
SUSB#_PWR POWER Control



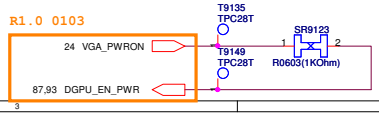
DSC#_PWR POWER(DGPU)



USBCHG#_PWR POWER



DSC_VGA_PWR POWER Control



<Variant Name>

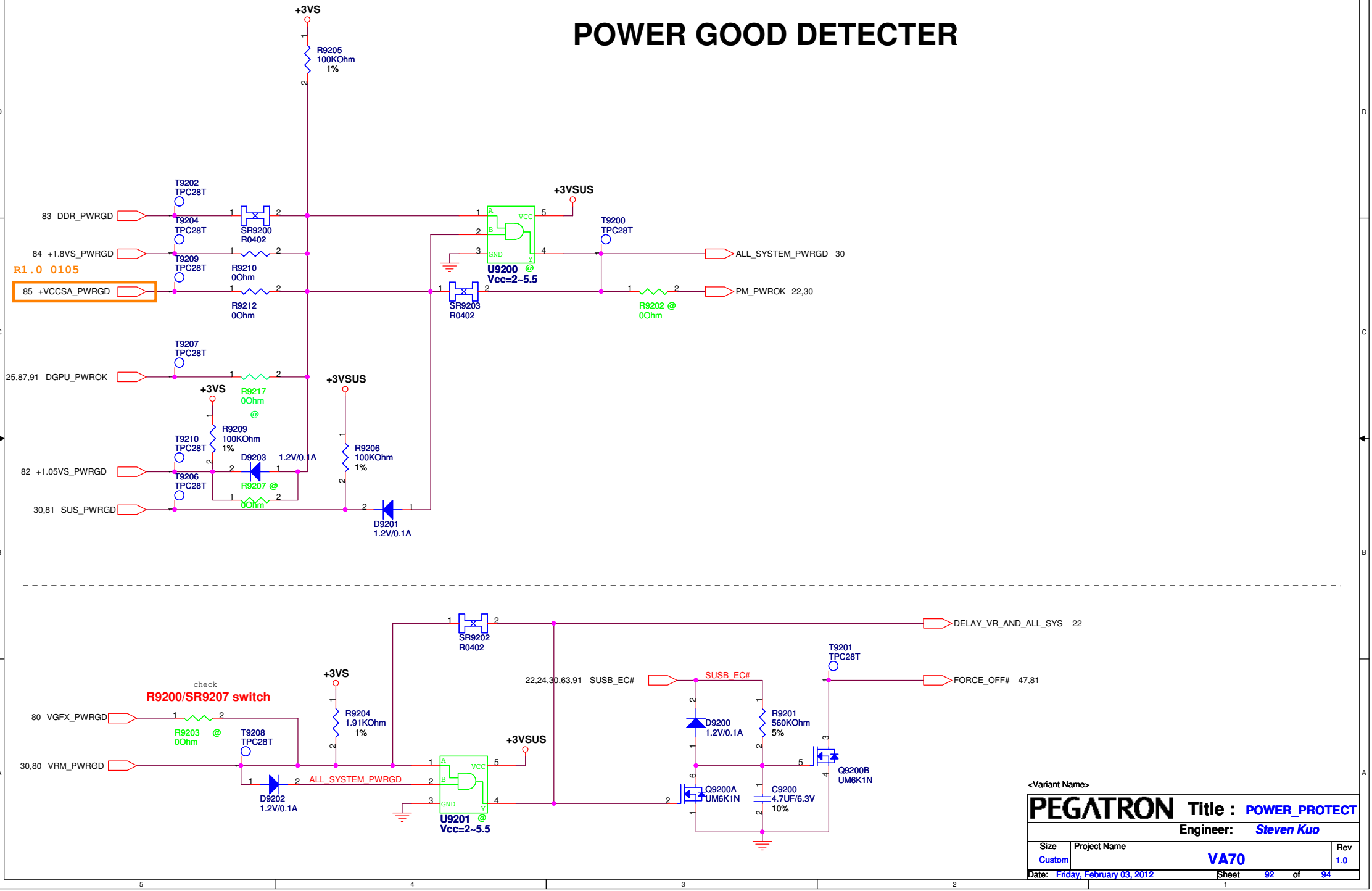
PEGATRON Title : POWER_LOAD SWITCH

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

Date: Friday, February 03, 2012 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

PEGATRON	Title : POWER_PROTECT	
	Engineer: Steven Kuo	
Size: Custom	Project Name: VA70	Rev: 1.0
Date: Friday, February 03, 2012	Sheet 92 of 94	

AC_BAT_SYS — AC_BAT_SYS 37,55,80,81,82,83,87,88

BAT_CON — BAT_CON 63,88

+5VA — +5VA 30,42,61,66,81,91

+3VA — +3VA 20,27,30,48,63,65,81,88

+5VO — +5VO 61,81,91

+3VO — +3VO 55,81,91

+1.8VO — +1.8VO 84

+1.5VO — +1.5VO 83,91

+1.05VO — +1.05VO 82,91

+12VSUS — +12VSUS 22,28,60,81,91

+5VSUS — +5VSUS 22,27,30,60,61,63,65,66,82,83,84,85,91

+3VSUS — +3VSUS 4,22,24,27,28,30,33,65,81,85,92

+12V — +12V 91

+5V — +5V 51,63,91

+3V — +3V 4,24,37,51,63,65,91

+1.5V — +1.5V 5,7,16,51,63,83

+12VS — +12VS 28,39,41,91

+5VS — +5VS 27,30,38,39,41,42,48,49,60,63,66,80,87,91

+3VS — +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92

+1.8VS — +1.8VS 7,25,26,63,84

+1.5VS — +1.5VS 26,53,55,63,91

+1.05VS — +1.05VS 26,27,63,80,82,87

+0.75VS — +0.75VS 16,17,63,83

+VCCSA — +VCCSA 7,85

+VCCP — +VCCP 3,4,6,7,25,26,27,37,47,63,82

+12VS_VGA — +12VS_VGA 91

+3VS_VGA — +3VS_VGA 63,70,72,74,75,87,91

+1.5VS_VGA — +1.5VS_VGA 63,71,75,76,77,91

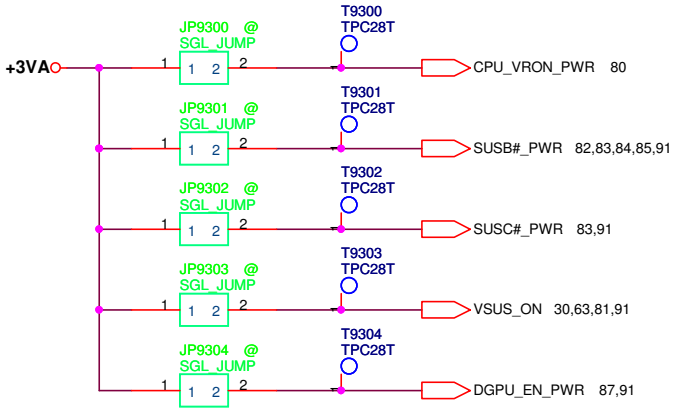
+1.05VS_VGA — +1.05VS_VGA 63,70,71,72,91

+VGA_VCORE — +VGA_VCORE 63,75,87

+VGFX_CORE — +VGFX_CORE 7,63,80

+VCORE — +VCORE 6,63,80

FOR POWER TEST



<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	A35	1.0

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